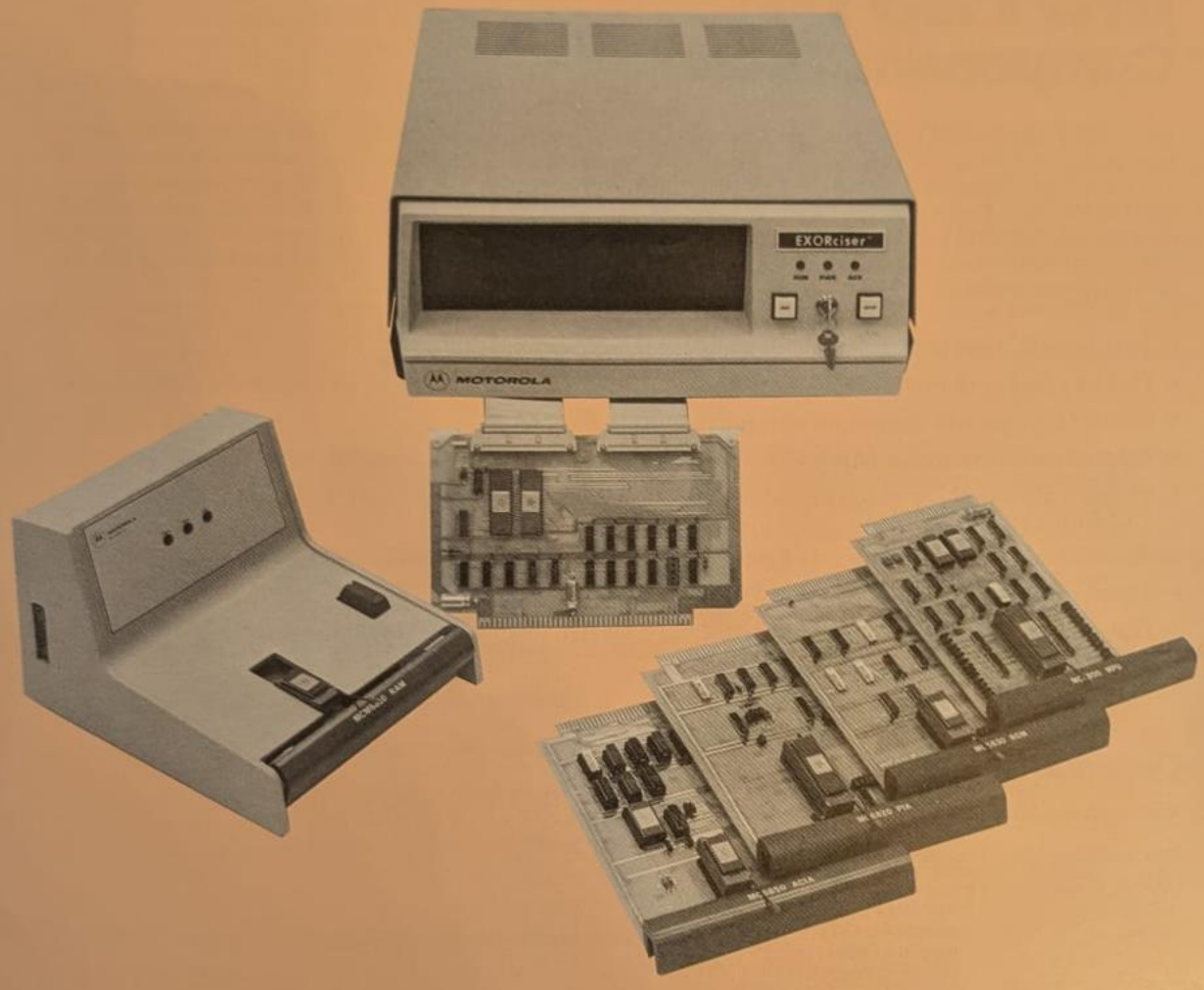
MOTOROLA MICROSYSTEMS



MEX68CT
MOTEST-I
Component Tester

ISSUE A

MEX68CT
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MOTEST-I (MEX68CT) is a dynamic LSI tester that provides the EXORciser with the capability of testing the M6800 microcomputer family of parts in an environment that closely approximates the end use conditions. Presently, MOTEST-I has the capability of testing the MC6800 Microprocessor Unit (MPU), MC6820 Peripheral Interface Adapter (PIA), MC6850 Asynchronous Communications Interface Adapter (ACIA), MCM6810 128 x 8 Bit Static Random Access Memory (RAM), and MCM6830 1024 x 8 Bit Read Only Memory (ROM). Using the Universal ROM card, additional TTL-compatible ROMs can also be accommodated.

- Functionally tests M6800 microcomputer family of parts in real time
- Can be adapted to test other devices: memories, TTL parts, CMOS parts, and other microprocessors
- One EXORciser will control up to eight test heads
- Uses internal EXORciser power (+5 Vdc) or external power (determined by user)
- Provides statistical log which indicates PART TYPE, TOTAL TESTED, TOTAL FAILED, and % GOOD for each test head
- Provides interlocking between test program and personality card in the test head
- Optional footswitch control
- Optional extender allows personality card to be located in environmental chamber for environmental testing
- PASS/FAIL indications

Ordering Information

When ordering MOTEST-I, the user selects the options he requires.

Part Number	Description
MEX68CT A,B,D	Component Tester Test Head (1) Control Card (1) Interface Cables (2) Executive Program (1)

Options

Part Number	Description
MEX68CT2 A,B,D	MPU (MC6800) Personality Card, Test Program
MEX68CT3 A,B,D	PIA (MC6820) Personality Card, Test Program
MEX68CT4 A,B,D	ACIA (MC6850) Personality Card, Test Program
MEX68CT5 A,B,D	ROM (MCM6830) Personality Card, Test Program
MEX68CT6	ROM Universal Personality Card, Test Program
MEX68CT7 A,B,D	RAM (MCM6810) Personality Card, Test Program
MEX68CT10	Footswitch

A Suffix – Cassette, B – Paper Tape, D – Diskette

Component Testing

Control is returned to the Executive Program due to either PASS or FAIL.

MPU Testing

The following tests are performed on the MPU:

- The test program is loaded into the two resident 128 byte RAMs.
- Control is transferred to the MPU under test, and the "instruction set" (1) is executed. Termination is a WAI causing BA to go true.
- The EXORciser looks for BA from the MPU under test or time out, whichever comes first.
- NMI and IRQ are independently pulled causing the MPU to go to another WAI in the program, depending upon the state of the interrupt mask described in the following step.
- Modification of the program changes the running address from $00XX_{16}$ to $55XX_{16}$. The instruction CLI is substituted for SEI on this pass.
- Assuming successful execution of the first pass, as evidenced by returning control to the EXORciser and reading the memory and comparing the results to known check sums, the program is modified.
- The program is now run again and the results checked.
- The program is again modifed to run at $2AXX_{16}$. The instruction SEI is exchanged for CLI on this pass.
- The program is now run again and the results checked.
- The instructions not previously executed, as described in footnote (1), are now run. These include stack and index register codes, subroutine jumps and returns flagged by the index register.
- Upon successful completion of the program that has just run, TSC is enabled by the EXORciser causing the MPU under test to execute the code in location $FFFF_{16}$.
- NMI is then enabled, vectoring the MPU to another WAI instruction.
- Memory is again checked for successful execution of the second program.

PIA Testing

The following tests are performed on the PIA:

- Test Reset Line clears all PIA registers.
- Test ability to read/write Data Direction Registers.
- Test A-Data Register as an output while driving B-Data Register as an input.
- Test A-side Chip Selects and B-side Write Enable.
- Test B-Data Register as an output while driving A-Data Register as an input.
- Test B-side Chip Selects and A-side Write Enable.
- Test three-state capability of CA2 and CB2.
- Test CA1 and CB1 as interrupt input lines.
- Test CA2 as an output line while CB2 is an input line.
- Test CB2 as an output line while CA2 is an input line.

ACIA Testing

The following tests are performed on the ACIA:

- Test Master Reset.
- Test ACIA for ability to transmit and receive data at 110 baud.
- Test ACIA for ability to transmit and receive data at 5200 baud.
- Test ACIA at different word lengths and parity selections using 500 kHz clock rate.
- Test for Transmit Interrupt and double buffering capability.
- Test Break.
- Test Ready to Send, RTS.
- Test Clear to Send, CTS.
- Test Data Carrier Detect, DCD.
- Test Receive Interrupt.
- Test Overrun Error.
- Test Framing Error.
- Test Chip Selects.
- Test False Start Bit Detection.
- Test Parity Error Detection.

RAM Testing

The following tests are performed on the RAM:

- Walking Address test.
- Bit pattern AA R/W test.
- Bit pattern 55 R/W test.
- Galloping Read test.
- Galloping Write test.
- Walking Bit Pattern tests.

  10000000 00100000 00001000 00000010
  01000000 00010000 00000100 00000001
- Test Chip Selects.

ROM Testing

The following tests are performed on the ROM:

- The message flag is tested. If the flag is a one, the ROM is read, and its contents are saved to be used as a reference pattern. The flag is then set to a zero. If the flag is a zero, the ROM is tested.

The following tests are then performed:

- The Chip Selects are enabled. The ROM is read, and its contents are compared to the reference pattern.
- One Chip Select at a time is disabled. The ROM is read to test the function of the respective Chip Select.

(1) The instruction set is incremented from 01 "NOP" to FF "STX". All undefined codes, index modification codes, JSR, RTI, stack or stack modification codes are omitted in the valid OP code file and tested separately.

MEX68CT MOTEST-I
General Description

The MOTEST-I system requires an EXORciser containing an MPU Module, Debug Module, Baud Rate Module, and the required memory. The memory size is determined by the number of device types being tested. MOTEST-I, itself, consists of a control card which plugs into the EXORciser, interface cables, test head, Executive program, test programs and a personality card designed for each particular part. One EXORciser will control up to eight test heads without any restriction on the mix of parts being tested. When setting up your test system, it is important to remember that each test head requires a control card and a set of interface cables to connect the test head to the EXORciser. To set up the system, the interface cables are connected to the control card, and the control card is then inserted into the EXORciser. The other ends of the interface cables are connected to the test head. If external voltages are required, they can be connected to the external power jack located on the side of the test head. To test a part, the user simply selects and inserts the particular personality card into the test head, loads the Executive and appropriate test program (using the LOAD function of EXbug) into the EXORciser, and MOTEST-I is ready to evaluate the device. The user now installs the device to be evaluated into the test socket located on the personality card, presses the TEST switch and monitors the indicators to see if the part has passed or failed.

System Software

MOTEST-I system software consists of one Executive program and a test program for each personality card.

EXECUTIVE – The Executive performs the function of initializing and polling the control cards for a start test interrupt, verifying the device/test program interlock, controlling power to device under test so that it can be installed and removed with power off, providing a statistical log on request, and providing a command structure to aid setup.

TEST PROGRAM – The test program, upon receiving control from the Executive program, performs the following functions: calculates the test device address, sets up the control PIAs to perform the test, and sequentially tests each parameter of the test device. Control is returned to the Executive program as a result of a PASS or FAIL indication.

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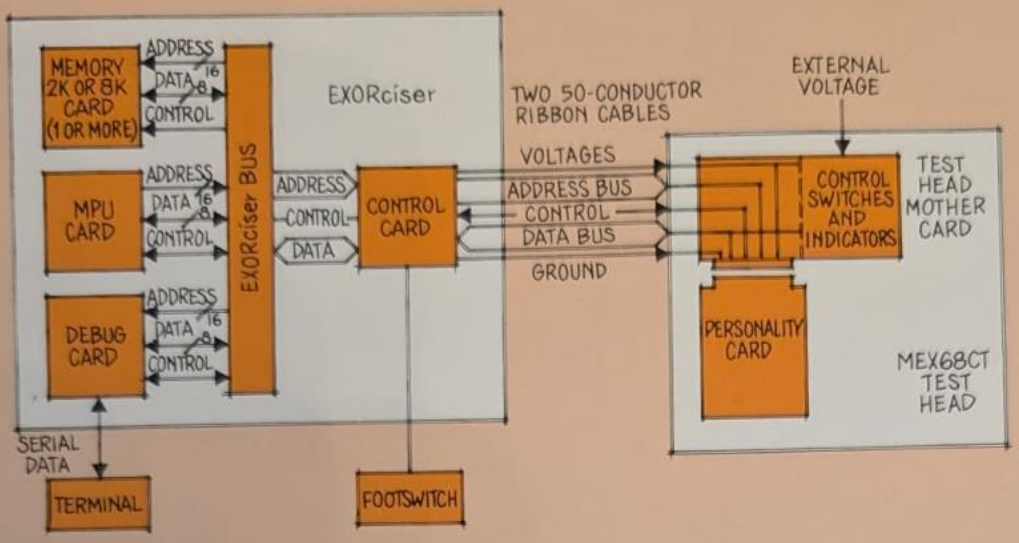

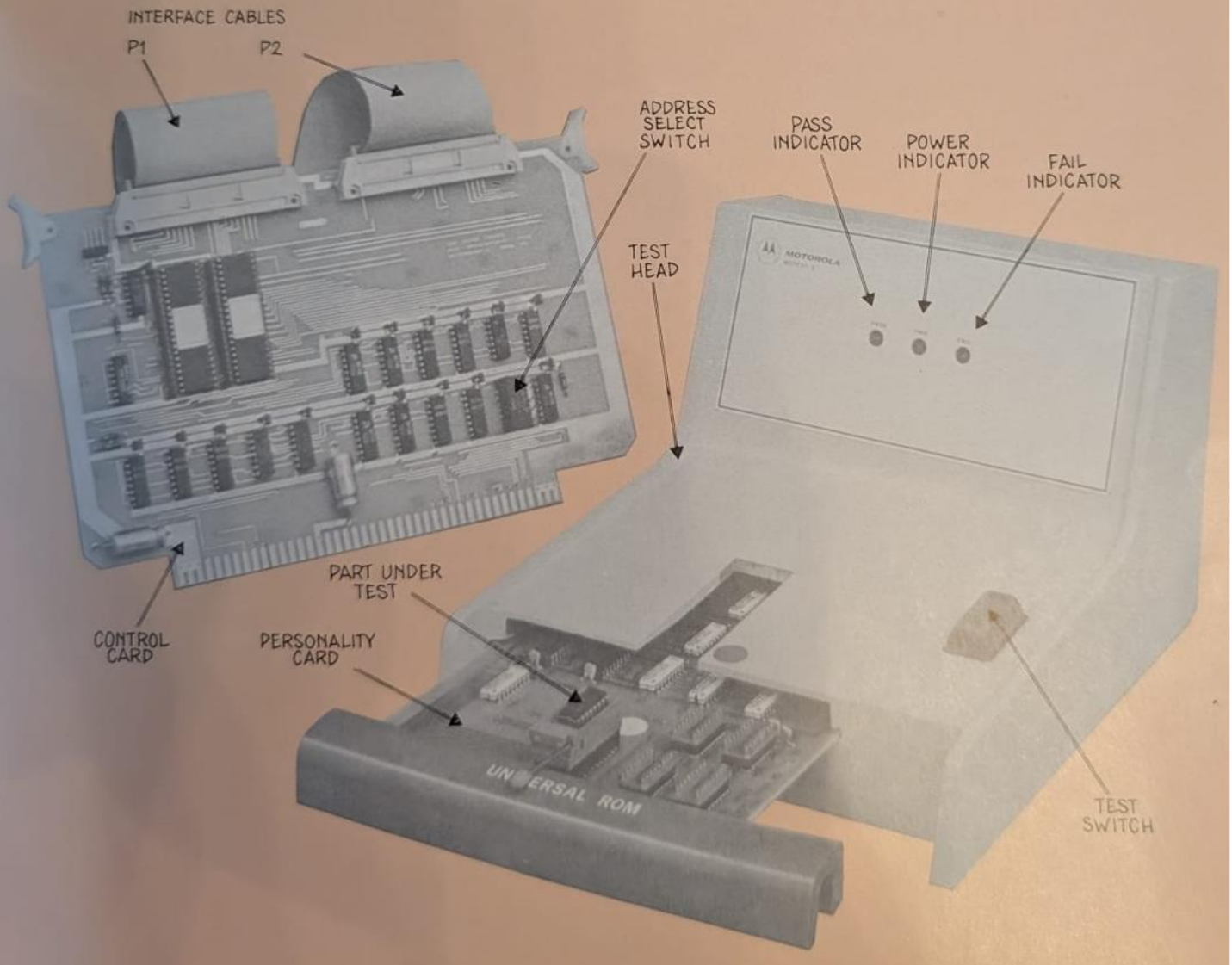

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