MOTOROLA Semiconductors

MEX6800

Advance Information

EXORciser
MPU MODULE

MPU MODULE

The MEX6800 MPU Module is the heart of both the EXORciser Debug system and the user's system under development. That is, the MPU Module provides both the system clock and the MC6800 Microprocessing Unit (MPU) for the EXORciser Debug and the user's system. The MPU Module also automatically initiates an EXORciser restart operation when power is first applied to the EXORciser.

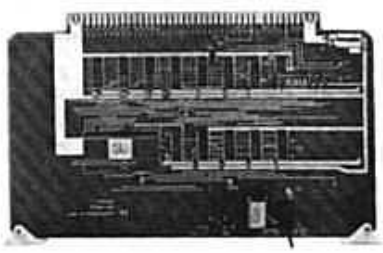
The clock circuit, in addition to generating the basic EXORciser timing signals, provides the EXORciser with the capability of refreshing dynamic memories and working with slow memories. The dynamic memories are refreshed on a cycle stealing basis. In working with slow memories, the MPU Module stretches the clock pulse to allow the two-way transfer of data.

The MC6800 Microprocessing Unit is an 8-bit parallel device capable of addressing 64K bytes of memory. It addresses its input and output devices as memory. The MPU provides the EXORciser with 72 variable length instructions and the capability of responding to real time interrupt signals. With the exception of the EXORciser clock, the system restart, and the Data Bus Enable signal (delayed), the MPU Module appears exactly like an MC6800 Microprocessing Unit with unlimited drive capability.

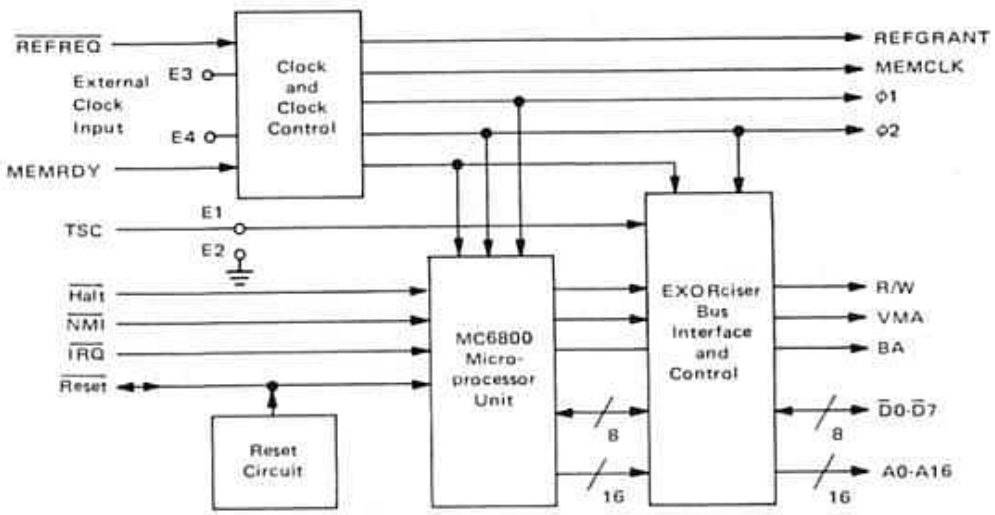
- Provides MPU and Clock for the EXORciser Debug and User's System
- Crystal-Controlled 1 MHz Clock
- Provisions for an External Clock Input
- Automatic Restart Capability
- Dynamic Refresh Capability on a Cycle Stealing Basis
- Capable of Working with Slow Memories Through Stretching the $\phi 2$ Clock Pulse

EXORciser

MPU MODULE



BLOCK DIAGRAM



MODULE SPECIFICATIONS

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Specification		Value
Memory Size Capability		65,536 bytes maximum
Word Size	Data Address Instruction	8 bits 16 bits 8, 16, or 24 bits
Instruction Set		72 variable length instructions
Interrupts		Maskable and non-maskable real-time interrupts Software interrupt
Clock Signal		1 MHz; provision for external clock between 100 kHz and 1 MHz
Input Control Signals Logic "0" Logic "1"		TTL Voltage Compatible 0.0-0.8 V 2.0-5.25 V
Address Bus and R/W Logic "0" Logic "1" Off-State Leakage Current		 0.0-0.5 V 2.4-5.25 V -40 μA
Data Bus Input Logic "0" Input Logic "1" Output Logic "0" Output Logic "1" Output Off-State Leakage Current		Three-state TTL voltage compatible 0.0-0.8 V (-200 μA at 0.4 V) 2.0-5.25 V (25 μA at 5.25 V) 0.0-0.5 V (40 mA at 0.5 V) 2.6-5.25 V (-10 mA at 2.6 V) 100 μA at 2.6 V
Output Control Signals Logic "0" Logic "1"		TTL voltage compatible 0.0-0.4 V 2.4-5.25 V
Operating Temperature		0 to 70°C
Power Requirements		5 Vdc at 700 mA
Dimensions Width Height Thickness		 9.75 in. 5.75 in. 0.062 in.

EXORciser INTERFACE SIGNALS

The MEX6800 MPU Interface Module interfaces directly with the EXORciser bus using the following signals. The MPU Module, through these signals, controls the operation of the EXORciser.

Data Bus ($\overline{D0}$-$\overline{D7}$) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bus drivers and receivers on the MPU Module are three state devices. The data bus drivers and receiver are in their off or high impedance state except when this module is performing a memory read or write operation.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three-state bus drivers.

Read/Write (R/W) – This MPU output signal indicates whether the MPU Module is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the module is halted, this signal will be in the read state.

Valid Memory Address (VMA) – This line, when high, indicates that the address on the bus is valid.

Memory Clock (MEMCLK) – This is the basic clock signal used by the MPU Module to generate its $\phi 1$ and $\phi 2$ non-overlapping clock signals.

Phase 1 ($\phi 1$) Clock – This signal is derived from the Memory Clock and is present during the MPU addressing time. This signal is controlled by the MPU Module.

Phase 2 (φ2) Clock – This signal also is derived from the Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module.

Bus Available (BA) – The Bus Available signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is low or the MC6800 MPU is in the WAIT state as the result of executing a WAI instruction. At such time, all the MPU Module three-state output drivers will go to their off state and other outputs to their normally inactive state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the WAIT state.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence.

Non-Maskable Interrupt (NMI) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

$\overline{\text{Reset}}$ – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when power is first applied to the EXORciser and each time the EXORciser's RESTART switch is actuated. This signal, in addition to resetting the module's MPU, is used to reset and initialize the rest of the EXORciser Debug and the user's system.

Three-State Control (TSC) – This input, when high, causes all of the MPU Module's Address Bus lines and R/W line to go to their off or high-impedance state. The Valid Memory Address signal will be forced low. The Data Bus is not affected by the Three-State Control. This signal is strapped to ground on this module, but is available for DMA.

$\overline{\text{Refresh Request}}$ ($\overline{\text{REFREQ}}$) – This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the φ1 and φ2 clock signals with φ1 high and, through the Refresh Grant command, instructs the initiating memory module to refresh itself.

Refresh Grant (REFGRANT) – The MPU Module, on receiving a $\overline{\text{Refresh Request}}$ input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Ready (MEMRDY) – This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the φ1 and φ2 clock signals with φ2 high. The initiating module, on completing its memory operation, returns the Memory Ready signal to a high level.

$\overline{\text{Halt}}$ – When this input is low, all activity in the MC6800 MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of φ1. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one φ1 clock pulse.