# MCM6832L

## Advance Information

### 2048 x 8-BIT READ ONLY MEMORY

The MCM6832 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel metal-gate technology. For ease of use, the device is compatible with TTL and DTL, and needs no clocks or refreshing because of static operation.

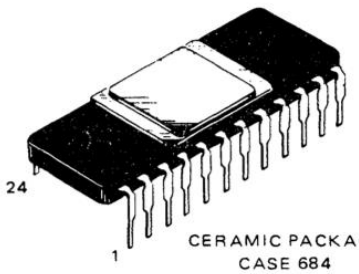
The memory is compatible with the M6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through a Chip Select input. The active level of the Chip Select input and the memory content are defined by the customer.

- Organized as 2048 Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Programmable Chip Select
- TTL Compatible
- Maximum Access Time = 550 ns

**MOS**

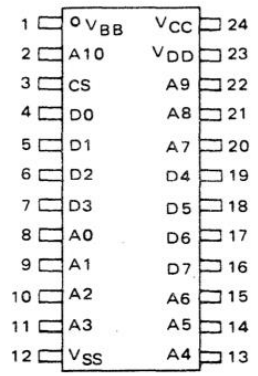
(N-CHANNEL, LOW THRESHOLD)

**2048 x 8-BIT READ ONLY MEMORY**




CERAMIC PACKAGE
CASE 684

PIN ASSIGNMENT

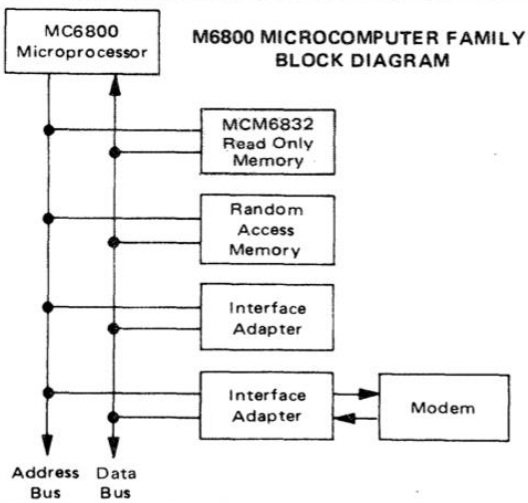



**ABSOLUTE MAXIMUM RATINGS[1]** (Referenced to $V_{SS}$)

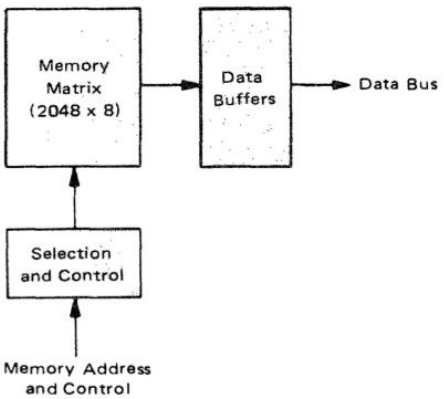
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltages | $V_{DD}$<br>$V_{CC}$<br>$V_{BB}$ | -0.3 to +15<br>-0.3 to +6.0<br>-10 to +0.3 | Vdc |
| Address/Control Input Voltage | $V_{in}$ | -0.3 to +15 | Vdc |
| Operating Temperature Range | $T_A$ | 0 to +70 | °C |
| Storage Temperature Range | $T_{stg}$ | -55 to +125 | °C |

Note 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM




MCM6832 READ ONLY MEMORY
BLOCK DIAGRAM




This is advance information and specifications are subject to change without notice.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

**(Full operating voltage and temperature range unless otherwise noted.)**

### RECOMMENDED DC OPERATING CONDITIONS (Referenced to $V_{SS}$ = Ground)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 11.4 | 12 | 12.6 | Vdc |
| | $V_{CC}$ | 4.75 | 5.0 | 5.25 | Vdc |
| | $V_{BB}$ | -5.25 | -5.0 | -4.75 | Vdc |
| Input High Voltage ($A_n$, CS) | $V_{IH}$ | 3.0 | – | $V_{CC}$ | Vdc |
| Input Low Voltage ($A_n$, CS) | $V_{IL}$ | -0.3 | – | 0.8 | Vdc |

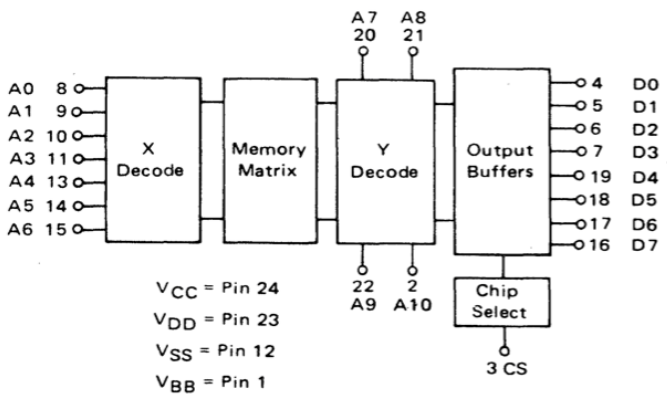
### DC CHARACTERISTICS

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Leakage Current ($A_n$, CS) ($V_{in}$ = 0 to 5.25 V) | $I_{in}$ | – | – | 10 | μAdc |
| Output Leakage Current (Three-State) ($V_O$ = 0.4 V to -2.4 V, CS = 0.4 V or $\overline{CS}$ = 2.4 V) | $I_{LO}$ | – | – | 10 | μAdc |
| Output High Voltage ($I_{OH}$ = -100 μA) | $V_{OH}$ | 3.7 | – | $V_{CC}$ | Vdc |
| Output Low Voltage ($I_{OL}$ = 1.6 mA) | $V_{OL}$ | 0 | – | 0.4 | Vdc |
| Supply Current (Chip Deselected or Selected) | $I_{DD}$ | – | – | 25 | mAdc |
| | $I_{CC}$ | – | – | 45 | mAdc |
| | $I_{BB}$ | – | – | 500 | μAdc |

### CAPACITANCE (Periodically Sampled Rather Than 100% Tested.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance ( f = 1 MHz) | $C_{in}$ | – | 5.0 | 7.5 | pF |
| Output Capacitance (f = 1 MHz) | $C_{out}$ | – | 5.0 | 10 | pF |

### BLOCK DIAGRAM



## AC CHARACTERISTICS

**(Full operating voltage and temperature unless otherwise noted. All timing with $t_r = t_f \leq 20$ ns; Load = 1 TTL Gate (MC7400 Series) biased to draw 1.6 mA; $C_L$ = 130 pF.)**

| Characteristic | Symbol | Min | Typ* | Max | Unit |
|---|---|---|---|---|---|
| Address Access Time | $t_{acc}$ | – | 320* | 550 | ns |
| Output Select Time | $t_{OS}$ | – | 175* | 300 | ns |
| Output Deselect Time | $t_{OD}$ | 30 | 100* | 150 | ns |

*Typical values measured at 25°C and nominal supply voltages.

**FIGURE 1 – AC TEST LOAD**

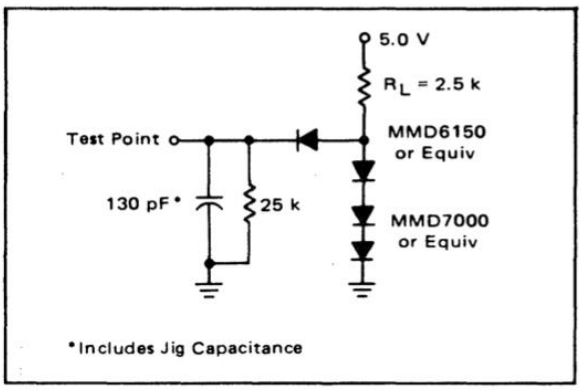
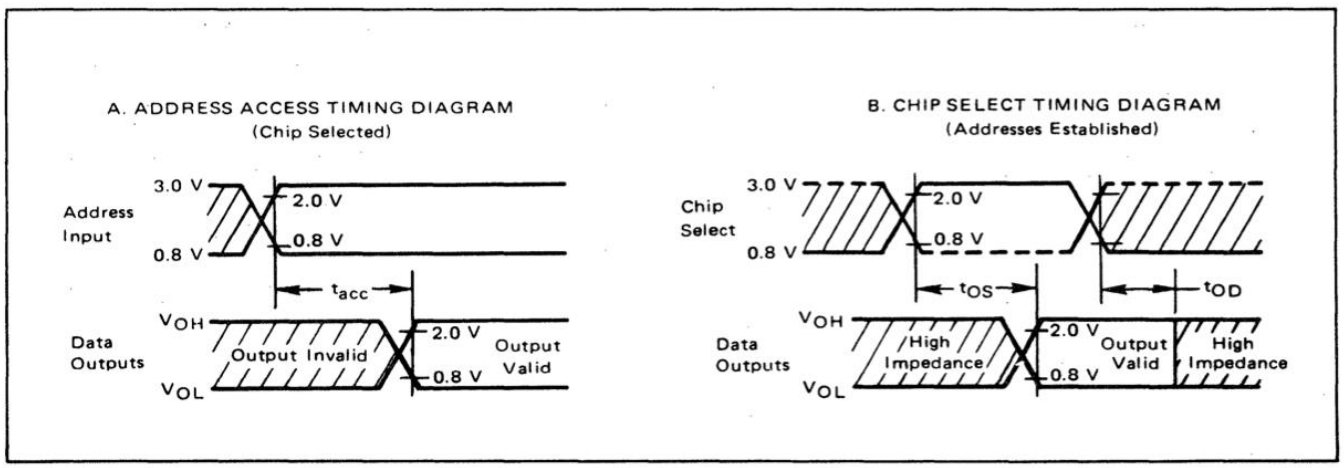



**FIGURE 2 – TIMING DIAGRAM**



## CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM6832, the customer may specify the content of the memory and the method of enabling the outputs.

Information on the general options of the MCM6832 should be submitted on an Organizational Data form such as that shown in Figure 4.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

1. Paper tape output of the Motorola M6800 Software.
2. Hexadecimal coding using IBM Punch Cards.

### PAPER TAPE

Included in the software packages developed for the M6800 Microcomputer Family is the ability to produce a paper tape output for computerized mask generation. The procedure for generating and verifying a system is shown in Figure 5. The assembler directives are used to control allocation of memory, to assign values for stored data, and for controlling the assembly process. The paper tape must specify the full 2048 bytes.

Note: Motorola can accept magnetic tape and truth table table formats. For further information, contact your local Motorola sales representative.

**FIGURE 3 – BINARY TO HEXADECIMAL CONVERSION**

| MSB D7 D3 | D6 D2 | D5 D1 | LSB D4 D0 | Hexadecimal Character |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | A |
| 1 | 0 | 1 | 1 | B |
| 1 | 1 | 0 | 0 | C |
| 1 | 1 | 0 | 1 | D |
| 1 | 1 | 1 | 0 | E |
| 1 | 1 | 1 | 1 | F |

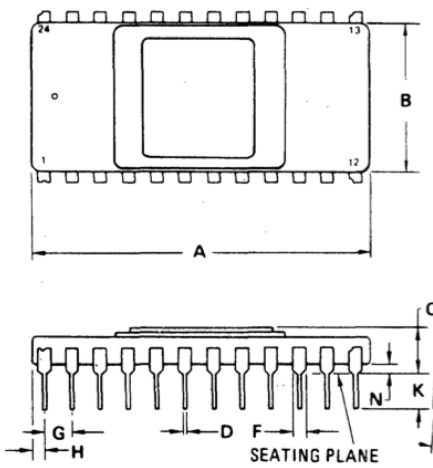
$0 = V_{OL}$
$1 = V_{OH}$

### IBM PUNCH CARDS

The hexadecimal equivalent (from Figure 3) may be placed on 80 column IBM punch cards as follows:

| Step | Column | |
|---|---|---|
| 1 | 12 | Byte "0" Hexadecimal equivalent for outputs D7 thru D4 (D7 = M.S.B.) |
| 2 | 13 | Byte "0" Hexadecimal equivalent for outputs D3 thru D0 (D3 = M.S.B.) |
| 3 | 14-75 | Alternate steps 1 and 2 for consecutive bytes. |
| 4 | 77-78 | Card number (starting 01) |
| 5 | 79-80 | Total number of cards (64) |

### PACKAGE DIMENSIONS




NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE WITH MAXIMUM MATERIAL CONDITION.
2. LEAD NO. 1 CUT FOR IDENTIFICATION, OR BUMP ON TOP.
3. DIM "L" TO INSIDE OF LEADS. (MEASURED 0.51 mm (0.020) BELOW PKG BASE)

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 29.34 | 30.86 | 1.155 | 1.215 |
| B | 12.70 | 14.22 | 0.500 | 0.560 |
| C | 3.05 | 3.94 | 0.120 | 0.155 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 0.89 | 1.40 | 0.035 | 0.055 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.89 | 1.40 | 0.035 | 0.055 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.68 | 0.115 | 0.145 |
| L | 14.86 | 15.87 | 0.585 | 0.625 |
| M | – | 15° | – | 15° |
| N | 0.51 | 1.14 | 0.020 | 0.045 |

CASE 684-04

FIGURE 4 – FORMAT FOR PROGRAMMING GENERAL OPTIONS

**ORGANIZATIONAL DATA**
**MCM6832 MOS READ ONLY MEMORY**

Customer:

Company _____

Part No. _____

Originator _____

Phone No. _____

Motorola Use Only:

Quote: _____

Part No.: _____

Specif. No.: _____

True Chip Select Options:

I. 1 ☐

II. 0 ☐

1 is most positive input
0 is most negative input

**FIGURE 5 – SYSTEM DESIGN AND VERIFICATION PROCEDURE**