MOTOROLA Semiconductors

M68SDT

Advance Information

BASIC EXORciser

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The basic EXORciser (M68SDT) consists of the MPU Module, the Debug Module, the Baud Rate Module, the Power Supply and the chassis. These modules are built around the M6800 Microcomputer Family of Parts (MC6800 Microprocessing Unit, MCM6810 Random Access Memory, MC6820 Peripheral Interface Adapter, MCM6830 Read Only Memory, and MC6850 Asynchronous Communication Interface Adapter devices).

The MPU Module incorporates the MC6800 Microprocessing Unit (MPU) and the system clock. This module serves a dual function in that it provides the MPU and clock for both the EXORciser Debug and the user's system. With the exception of the EXORciser clock, the system restart and the DBE signal (delayed), the MPU Module appears exactly like the MC6800 Microprocessing Unit with unlimited TTL bus drive capability. The MPU is an 8-bit parallel device capable of addressing 65,536 bytes of memory. In addition, the MPU addresses its input and output devices as memory. The MPU also provides the EXORciser with 72 variable length instructions and the capability of responding to real time interrupt signals.

The Debug Module provides the EXORciser with the capability to evaluate and debug the user's program. The three MCM6830 ROM memories on this module contain the EXbug Firmware that provides the EXORciser with its unique software control features. The module also has two MCM6810 RAM memories to provide a scratch-pad memory to the EXbug Firmware.

The Debug Module working with the Baud Rate Module provides the EXORciser with eight standard baud rates between 110 and 9600 Baud. These modules also interface the EXORciser with a TTY or RS-232C compatible terminal and provide a reader control signal for remote control of modified manual TTY terminals.

The Power Supply provides the EXORciser with the +5 Vdc, +12 Vdc, and −12 Vdc power sources to support a full EXORciser rack of modules.

The chassis is capable of holding 14 plug-in modules. The Power Supply and Baud Rate Modules are not plug-in modules but mount directly to the chassis. Two versions of the chassis are available — the rack mounted version and the table top version.

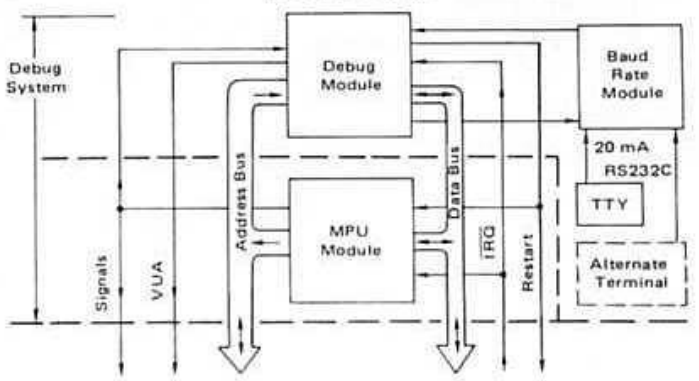
BASIC EXORciser

EXORciser

DIMENSIONS

Table Top Model	
M68SDT-T	
Width	19.25 in.
Depth	17.50 in.
Height	7.00 in.
Rack Mounted Model	
M68SDT-R	
Width	19.00 in.
Depth	17.00 in.
Height	7.00 in.

BLOCK DIAGRAM



BASIC EXORciser SPECIFICATIONS

Specification	Value
Power Requirements	95-135/205-250 Vac 47-420 Hz, 250 W
Word Size Data Address Instruction	 8 bits 16 bits 8, 16, and 24 bits
Memory Capability	65,536 bytes
Instruction Set	72 variable length instructions
Clock Cycle Time	Selectable; 1 μs crystal control clock or an external clock between 1 μs and 10 μs
Interrupt	Maskable real time interrupt
Data Terminal Interface Characteristics Baud Rates (Switch selectable) Signal Characteristics Reader Control Signal	 110, 150, 300, 600, 1200, 2400, 4800, and 9600 TTY (20 mA neutral current loop) or EIA RS-232C compatible Control signal for TTY devices modified for external control
Operating Temperature	0 to 55°C

EXORciser OPTIONS

The M6800 EXORciser derives its flexibility from its optional hardware, modules, and software. Two models of the EXORciser are available – a rack mounted model, and a table top model. When ordering, use the appropriate part number. In addition, specify the kit number for proper installation in the chosen location.

M68SDT-T	EXORciser, Table Top Model
M68SDT-R	EXORciser, Rack Mounted Model
MEX68TT	Table Top Kit
MEX68RK	Rack Mounting Kit

Optional assemblies permit the user to adapt his EXORciser to various system configurations, with memory size and input/output configuration selected to meet system needs. The optional modules include:

- MEX6812-1 2K Static RAM Module
- MEX6815-1 8K Dynamic RAM Module
- MEX6820 Input/Output Module
- MEX68IC I/O Flatribbon Interconnection Cable
- MEX68WW Universal Wirewrap Module
- MEX68XT Extender Module

Motorola supplies a variety of software programs to support the M6800 Microcomputer Family of Parts. These programs include Cross-Assemblers and Editors, Simulators, Build-Virtual Machine, and Help programs as well as the EXORciser Resident Editor and Assembler programs.

EXbug FIRMWARE

The EXbug Firmware is an integral part of the EXORciser, which provides system development program capability for debugging both the system hardware and software by enabling the user to perform the following functions:

- Load data into the EXORciser
- Verify that the data in the EXORciser or on tape is valid
- Search a tape for a specific file
- Print the contents of the memory
- Punch (record) the contents of the memory on tape
- Perform the MAID (Motorola Active Interface Debug) functions

The MAID functions enable the EXORciser to:

- Examine and, if required, change the contents in a memory location
- Examine and, if required, change the data in an MPU register
- Calculate the offset in the relative addressing mode
- Insert, display, and remove breakpoints in a user's program
- Free run or trace through a user's program under MAID control
- Stop the user's program on a specific program step
- Provide an oscilloscope trigger pulse at a selected program step
- Search memory for a specific bit pattern
- Perform decimal-octal-hexadecimal conversions

EXORciser BUS SIGNALS

The EXORciser bus interfaces the MPU Module with other modules being used in the EXORciser. This bus permits the EXORciser to be configured to meet a user's specific application.

Data Bus ($\overline{D0}$-$\overline{D7}$) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module and the selected memory location. The data bus drivers on the modules are three-state logic devices.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the MPU memory address to the selected memory location. The MPU Module controls the operation of these lines through its three-state bus drivers.

Read/Write (R/W) – This MPU output signal indicates whether the MPU Module is performing a memory read (high) or write (low) operation. The normal standby state of this line is read (high). Also, when the MC6800 MPU on the module is halted, this signal will be in the read state.

Valid Memory Address (VMA) – This line, when high, indicates that the address on the bus is valid.

Valid User's Address (VUA) – This line, when high, indicates that the address on the address bus is valid and the EXORciser is not addressing its EXbug program.

Memory Clock (MEMCLK) – This is the basic clock signal used by the MPU Module to generate its $\phi1$ and $\phi2$ non-overlapping clock signals.

Phase 1 ($\phi1$) Clock – This signal is derived from the Memory Clock and is present during the MPU addressing time. This signal is controlled by the MPU Module.

Phase 2 ($\phi2$) Clock – This signal also is derived from the Memory Clock and used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU Module.

Bus Available (BA) – The Bus Available signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is low or the MC6800 MPU is in the WAIT state as the result of executing a WAI instruction. At such time, all the MPU Module three-state output drivers will go to their off state and other outputs to their normally inactive state. An interrupt command or actuating the ABORT or RESTART switch removes the MPU from the WAIT state.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence.

$\overline{\text{Non-Maskable Interrupt}}$ ($\overline{\text{NMI}}$) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the MC6800 MPU. The MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, the MPU will begin its non-maskable interrupt routine.

$\overline{\text{Reset}}$ – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when power is first applied to the EXORciser and each time the EXORciser's RESTART switch is actuated. This signal, in addition to resetting the module's MPU, is used to reset and initialize the rest of the EXORciser.

Three-State Control (TSC) – This input, when high, causes all of the MPU Module's Address Bus lines and R/W line to go to their off or high-impedance state. The Valid Memory Address and Valid User's Address signal will be forced low. The Data Bus is not affected by the Three-State Control. This signal is initially jumpered to ground on the MPU Module.

$\overline{\text{Refresh Request}}$ ($\overline{\text{REFREQ}}$) – This signal, when low, initiates a memory refresh operation. The MPU Module, on receiving this input, stops generating the $\phi1$ and $\phi2$ clock signals with $\phi1$ high and, through the Refresh Grant command, instructs the initiating memory module to refresh itself.

Refresh Grant (REFGRANT) – The MPU Module, on receiving a $\overline{\text{Refresh Request}}$ input, generates a Refresh Grant signal to instruct the initiating module to refresh itself.

Memory Ready (MEMRDY) – This signal enables the MPU Module to work with slow memories. The MPU Module, on receiving a low level Memory Ready input, stops generating the $\phi1$ and $\phi2$ clock signals with $\phi2$ high. The initiating module, on completing its memory operation, returns the Memory Ready signal to a high level.

$\overline{\text{Halt}}$ – When this input is low, all activity in the MC6800 MPU will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be high, Valid Memory Address and Valid User's Address will be low, and all other three-state lines will be in their off or high-impedance state.

Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of $\phi1$. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one $\phi1$ clock pulse.

Refresh Clock (REFCLK) – This signal is generated by the dynamic memory module being used as the master refresh module. This signal is used to initiate a memory refresh operation on the dynamic modules functioning as slave refresh modules.

$\overline{\text{Stand By}}$ ($\overline{\text{STDBY}}$) – This line is a low level during a power-fail condition and a high level during normal EXORciser operation.

BUS CONTROL

It is possible for a module other than the MPU Module to gain control of the bus. This module would place a low level $\overline{\text{Halt}}$ on the bus and monitor the Bus Available signal. When the MPU Module completes the instruction it is performing, it generates a high level Bus Available signal. The module requesting control of the bus now must pull the Three-State Control line low, forcing the MPU Module address bus drivers to their high-impedance state. The requesting module now has control of the EXORciser bus until it elects to relinquish control.