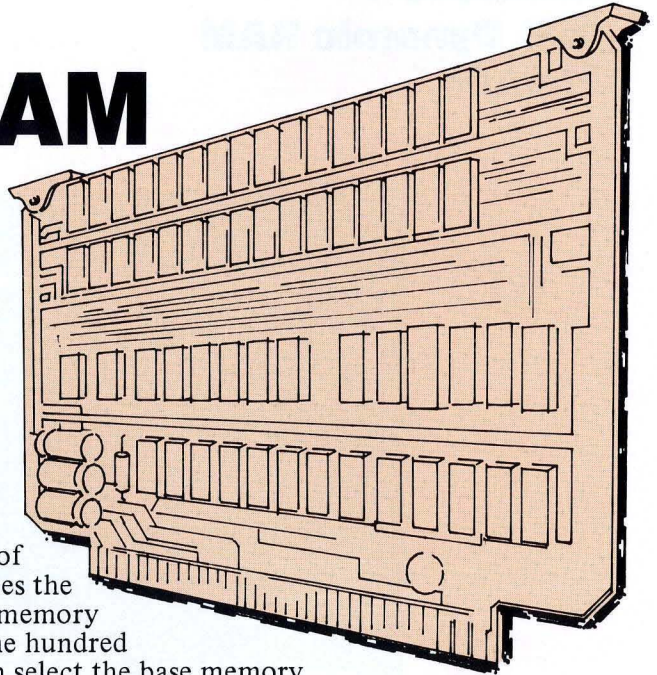




MEX6816-1

16K Dynamic RAM Module



- 16,384 x 8 bits of dynamic NMOS memory in one array
- Switch selectable base memory address for the memory array
- Cycle stealing memory refresh operation
- Optional even parity capability (consult factory)
- TTL voltage compatible
- Bus drive capability

The MEX6816-1 16K Dynamic RAM Module, consisting of 16 MCM6604L2 N-Channel MOS memory devices, provides the EXORciser with 16,384 bytes of dynamic memory. This memory is organized into one 16K memory array and simulates one hundred twenty-eight 128 x 8 bit MCM6810A RAMs. The user can select the base memory address for this array through setting the base memory address switches.

The address multiplexer in a refresh operation selects the memory location to be refreshed. During normal operation this circuit transfers its six address inputs to the EXORciser bus buffer. The EXORciser bus buffer latches its address input. The address decoder determines when the MPU is addressing its memory array and enables the control logic circuits. The control logic now decodes its control and timing inputs and determines the module's operation. Working with the EXORciser bus buffer, it controls the address multiplexing required by the MCM6604L2 devices. The control logic also decodes the Read/Write command and determines whether the module is to perform a memory read or memory write operation.

The control logic initiates a memory refresh operation once every 32 μ s and the module refreshes its memory on a cycle stealing basis.

The optional parity circuit generates a parity bit during a memory write operation and checks that data during a memory read operation. On detecting a parity error, the circuit generates the PARITY ERROR and PARITY ERROR flag signals. Consult the factory for details on this option.

Specifications

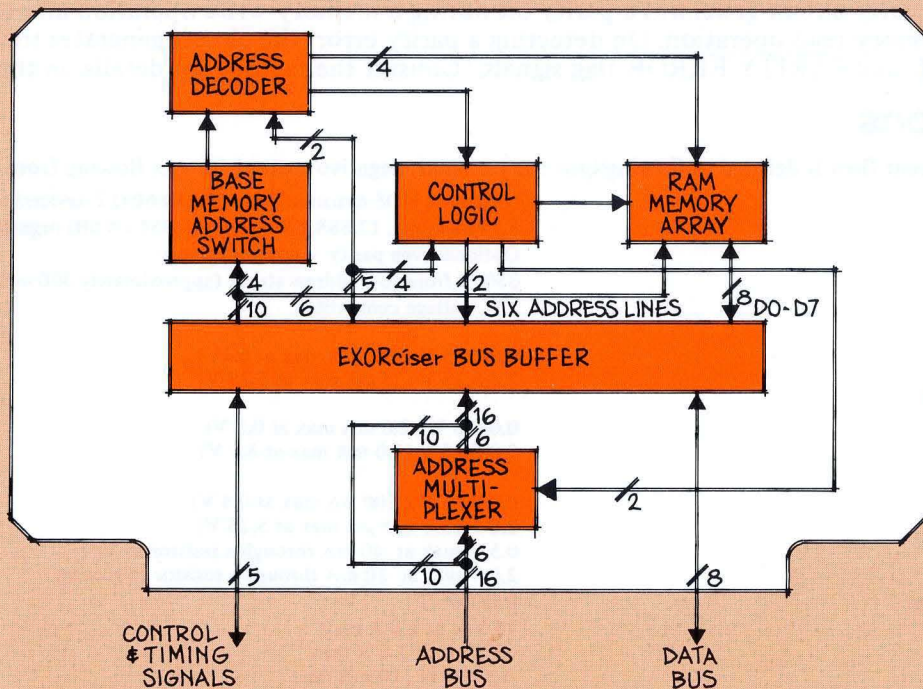
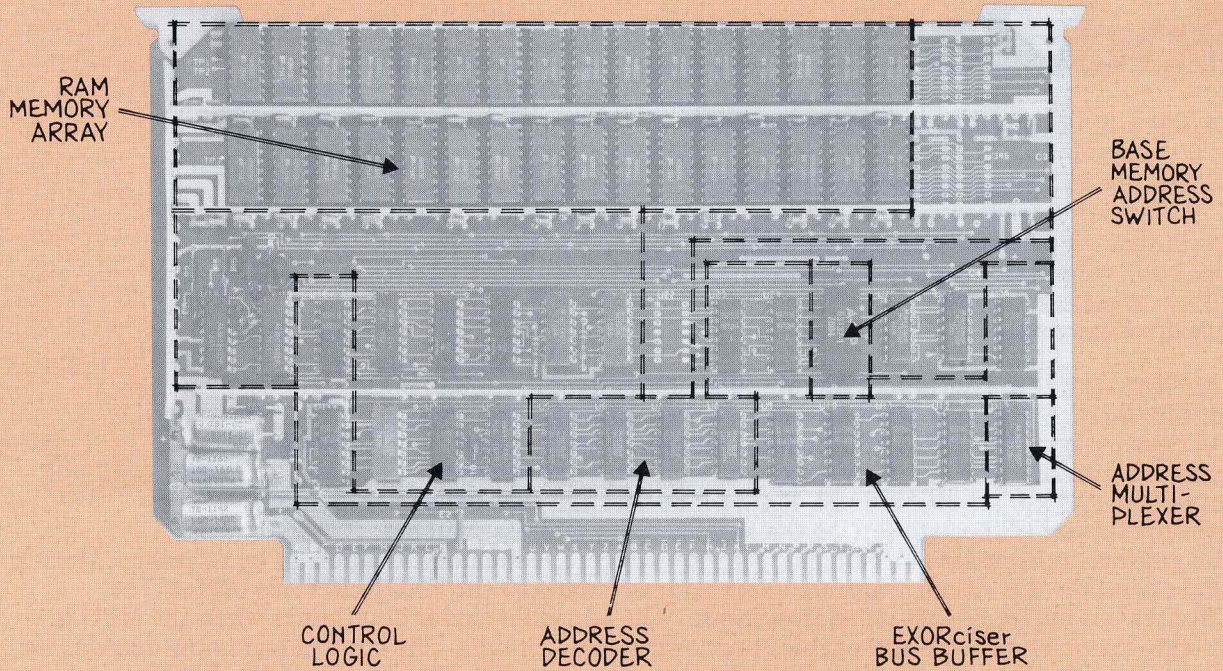
(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Memory Type	N-channel MOS dynamic RAM (MCM6604L2 devices)
Memory Organization	8,192 x 8 bits, 12,888 x 8 bits, or 16,384 x 8 bits organized into one array
Parity	Optional even parity – consult factory
Read Access Time	350 ns from row address strobe (approximately 300 ns from memory clock)
Input Signals	TTL voltage compatible
Control Lines	
Logic "0"	0.0-0.85 V (-200 μ A max at 0.4V)
Logic "1"	2.0-5.25 V (25 μ A max at 5.25 V)
Address	
Logic "0"	0.0-0.8 V (-2.0 mA max at 0.5 V)
Logic "1"	2.0-5.25 V (1.0 mA max at 5.5 V)
Data Bus	
Input Logic "0"	0.0-0.85 V (-200 μ A max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μ A max at 5.25 V)
Output Logic "0"	0.5 V max at -40 mA through a resistor to V_{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Operating Temperature	0 to 70° C
Power Requirements	+5 Vdc at 1.5 A max +12 Vdc at 1.6 A max -12 Vdc at 110 mA max
Physical Dimensions	
W x H x T	9.75 x 5.75 x 0.062 in.

MEX6816-1

16K Dynamic RAM Module

Option



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