MOTOROLA

MC6855

Product Preview

HMOS
(HIGH-DENSITY, N-CHANNEL
SILICON-GATE)

MC6855 SERIAL DIRECT MEMORY ACCESS PROCESSOR

The Serial Direct Memory Access Processor is **intended** as a high-speed serial link between MPU's or other intelligent controllers. This device can automatically transfer data to or from memory and receive or transmit that data over a serial link. Using bit oriented protocols (i.e., SDLC, HDLC, X.25), the SDMAP is capable of handling multidrop, point-to-point, or loop configurations in a full or half duplex environment. Bit rates of up to 4 MHz full duplex can be used. The Data Link is configured with a primary SDMAP connected to one or more secondary SDMAP's. The primary station (SDMAP and its associated local MPU) has responsibility for the data link control, such as mode of operation and polling of the secondary SDMAP's. The secondary stations which are relatively transparent to the local MPU will respond only to link commands from the primary station. Each SDMAP has the ability to respond to link-level commands with automatic responses or station status and handle link level error recovery without intervention by the local MPU.

An internal DMA controller is contained in the SDMAP and is capable of handling both a transmit and receive channel simultaneously. The DMA controller is transparent to the user. The local MPU only needs to write the location of a parameter table to the SDMAP. This parameter table contains the start address, message length, type of message, etc. The SDMAP automatically reads and loads the parameters into it's internal registers and then starts to transmit (or receive) data.

The SDMAP contains 7 control registers and 3 status registers. The control registers are used to configure the SDMAP, control reception and transmission of frames, and selectively mask interrupts. The status registers are used to monitor link activity, error conditions, and status of the SDMAP.

Other registers are included for local and group station addresses; test; I-frame counts (SDLC secondary only); and pointer registers used to define blocks of frames to transmit and blocks of receive buffers.

- Up to 4 MHz Bit Rate
- External Data Recovery
- External Clocks
- DMA Chaining
- Automatic Processing of a Subset of SDLC Commands
- HDLC/SDLC Protocols
- Full/Half Duplex Operation
- DMA Capability
- Normal or System Address Detection
- MC6809 Compatibility
- NRZ Operation
- Internal Byte Synchronization
- Point-to-Point Mode
- Multidrop Mode
- Loop Mode
- Separately Powered Pass-Through Logic (Loop Mode)

MPU INTERFACE PINS

Power – The SDMAP uses a single supply with two pins dedicated to +5 V and two pins for ground.

$\overline{\text{RESET}}$ – The $\overline{\text{RESET}}$ pin is an input used to reset the SDMAP and place it in the Power-On-Reset mode.

R/$\overline{\text{W}}$ (Read/Write) – R/$\overline{\text{W}}$ determines the direction of data transfers on the data bus for register or DMA accesses.

DATA TRANSFERS

When DMAGNT is asserted and the DMAREQ was generated by the SDMAP, the R/W pin is generated as an output. The condition of the R/W pin (low or high) is dependent upon the direction of data as determined by the SDMAP. When DMAGNT is low, R/W is an input controlled by the external processor and determines the direction of data transfers to or from the SDMAP registers.

$\overline{\text{IRQ}}$ (Output) – $\overline{\text{IRQ}}$ will be set low by the SDMAP to interrupt the MPU.

$\overline{\text{CS}}$ (Chip Select Input) – The $\overline{\text{CS}}$ input, in conjunction with the E input, is used to enable data transfers on D0-D7. E must be a high level and $\overline{\text{CS}}$ must be a low level to enable the transfer. The DMA Grant input being a high level performs a similar function as $\overline{\text{CS}}$ being a low level while in the DMA mode. $\overline{\text{CS}}$ is invalid during a DMA cycle.

E Clock (Input) – The E input to the SDMAP causes data transfers to occur between the SDMAP and the system controlling the SDMAP (MC6809 MPU, etc.).

Q (Quadrature Clock Input) – Q is an input to the SDMAP which precedes E by 90 degrees. It is used as an internal timing signal.

$\overline{\text{DMAR}}$ (DMA Request Output) – The $\overline{\text{DMAR}}$ is developed at the rising edge of Q to request the bus for data transfer. $\overline{\text{DMAR}}$ is dropped during Q.

DMAGNT (DMA Grant Input) – DMAGNT goes active on the falling edge of E placing the MPU bus in a 3-state mode and allowing the requesting device to become a bus master. DMAGNT takes the place of $\overline{\text{CS}}$ when in a DMA operation.

A0-A15 (Address Bus Bidirectional) – A0-A15, in conjunction with the R/$\overline{\text{W}}$ input, are used to select one of the MPU accessible registers in the SDMAP for programmed data transfer.

During any DMA operation A0-A15 are ignored as register select inputs and are used only as outputs to select the proper memory location.

D0-D7 (Data Bus Bidirectional) – The 8 bidirectional data lines allow the transfer of data between the SDMAP and the controlling system.

MCLK – The MCLK input supplied to the SDMAP is a crystal controlled 8 MHz clock used to supply the internal timing of the SDMAP.

$\overline{\text{MRDY}}$ (Memory Ready Output) – $\overline{\text{MRDY}}$ is output by the SDMA to stretch the falling edge of E during a register read or write operation to allow time for the data to be stable on the data bus prior to the falling edge of E.

$\overline{\text{DMAVMA}}$ (DMA Valid Memory Address Output) – $\overline{\text{DMAVMA}}$ goes low at the beginning of a DMA cycle to allow time for one controlling device to release the bus and another device to become the bus master. $\overline{\text{DMAVMA}}$ goes to zero on the rising edge of DMAGNT and returns to a one state on the next falling edge of E. It is during this time that address lines are allowed to switch.

TDATA (Transmit Data Output) – TDATA is the serial bit stream sent by the SDMAP in a synchronous format. TDATA is shifted out in an NRZ format on the negative edge of TXCLK.

TXCLK (Transmit Clock Input) – TXCLK is an input to the SDMAP generated by an external crystal oscillator source. This input takes standard TTL levels and is a X1 input.

RDATA (Receive Data Input) – RDATA is the serial bit stream received by the SDMAP in a synchronous format. The RDATA is synchronized externally to the RXCLK and is strobed into the SDMAP on the positive edge of the clock. The SDMAP requires the data to be input in an NRZ data format.

RXCLK (Receive Clock Input) – RXCLK is an input to the SDMAP generated by an external crystal oscillator source. It is a standard TTL level externally synchronized to the receive data and strobes the data into the SDMAP on the positive edge of the X1 Receive Clock.

$\overline{\text{RTS}}$ (Request to Send Output) – The $\overline{\text{RTS}}$ pin, when used in systems requiring modems, signals the modem to turn on the transmit carrier and initiate the return of $\overline{\text{CTS}}$. In systems not requiring modems, $\overline{\text{RTS}}$ is used as needed to control the flow of data on the serial line.

$\overline{\text{CTS}}$ (Clear to Send Input) – In systems using modems, $\overline{\text{CTS}}$ is a function of $\overline{\text{RTS}}$ and the modem's requirements for line turnaround. In systems not using modems, $\overline{\text{CTS}}$ is a function of $\overline{\text{RTS}}$ or $\overline{\text{RTS}}$ and an external delay circuit. No data is transmitted by the SDMAP until $\overline{\text{CTS}}$ is true.