



# MOTOROLA

# MC6822

## Product Preview

### INDUSTRIAL INTERFACE ADAPTER

The MCM6822 Industrial Interface Adapter (IA) provides the universal means of interfacing industrial peripheral equipment with the MC6800 Microprocessor Unit (MPU). This device is capable of interfacing the MPU with industrial peripherals through two 8-bit bidirectional peripheral parts and four control lines. No external logic is required for interfacing with most peripheral devices. Due to the open-drain design, Peripheral Ports A and B, as well as the peripheral control lines (CA1, CA2, CB1, CB2) can be pulled-up externally to 18.0 V maximum. The recommended operating voltage range for these ports is between 0 and 15 volts. Thus, the IIA can directly interface with 15 V CMOS (no level shifters are required). The IIA is also ideal for industrial applications when increased noise margins are required.

The functional configuration of the IIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Ports for Interface with Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- Open Drain Peripheral Lines Capable of Interfacing with Industrial Equipment
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on All Peripheral Lines
- Pin Compatible with MC6821 PIA
- TTL-Compatible Data Bus
- Fully Static Operation

## MOS

(N-CHANNEL, SILICON-GATE DEPLETION LOAD)

### INDUSTRIAL INTERFACE ADAPTER



L SUFFIX  
CERAMIC PACKAGE  
CASE 715

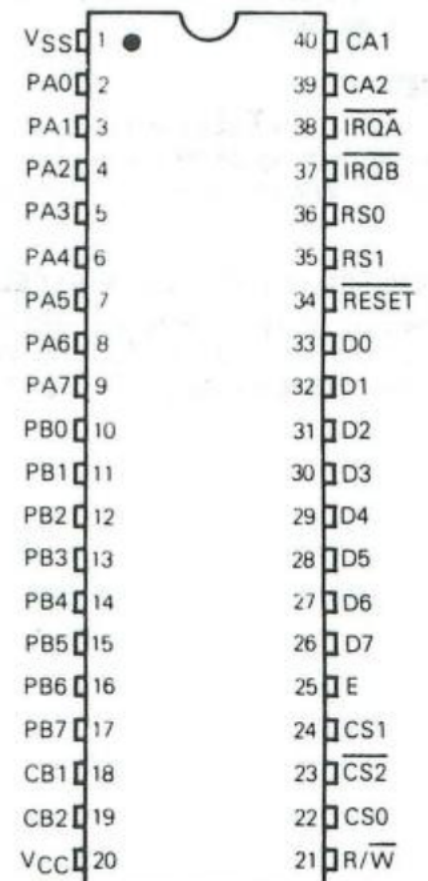


S SUFFIX  
CERDIP PACKAGE  
CASE 734



P SUFFIX  
PLASTIC PACKAGE  
CASE 711

### PIN ASSIGNMENT



## I/A INTERFACE SIGNALS FOR MPU

The I/A interfaces with the MC6800 MPU via an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line, and reset line. These signals, in conjunction with the MC6800 VMA output, permit the MPU to have complete control over the I/A. VMA should be utilized in conjunction with an MPU address line into a chip select of the I/A.

### I/A BIDIRECTIONAL DATA (D0-D7)

The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the I/A. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an I/A read operation. The Read/Write line is in the Read (high) state when the I/A is selected for a Read operation.

### I/A ENABLE (E)

The enable pulse, E, is the only timing signal that is supplied to the I/A. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the MC6800  $\phi 2$  Clock.

### I/A READ/WRITE (R/ $\overline{W}$ )

This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the I/A Read/Write line enables the input buffers and data is transferred from the MPU to the I/A by the E signal if the device has been selected. A high on the Read/Write line sets up the I/A for a transfer of data to the bus. The I/A output buffers are enabled when the proper address and the enable pulse E are present.

### $\overline{RESET}$

The active low  $\overline{RESET}$  line is used to reset all register bits in the I/A to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

### I/A CHIP SELECT (CS0-CS1 AND $\overline{CS2}$ )

These three input signals are used to select the I/A. CS0 and CS1 must be high and  $\overline{CS2}$  must be low for selection of the device. Data transfers are then performed under the con-

trol of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

### I/A REGISTER SELECT (RS0 AND RS1)

The two register select lines are used to select the various registers inside the I/A. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

### INTERRUPT REQUEST ( $\overline{IRQA}$ AND $\overline{IRQB}$ )

The active low Interrupt Request lines ( $\overline{IRQA}$  and  $\overline{IRQB}$ ) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the I/A which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each I/A for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the I/A is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

EXPANDED BLOCK DIAGRAM

