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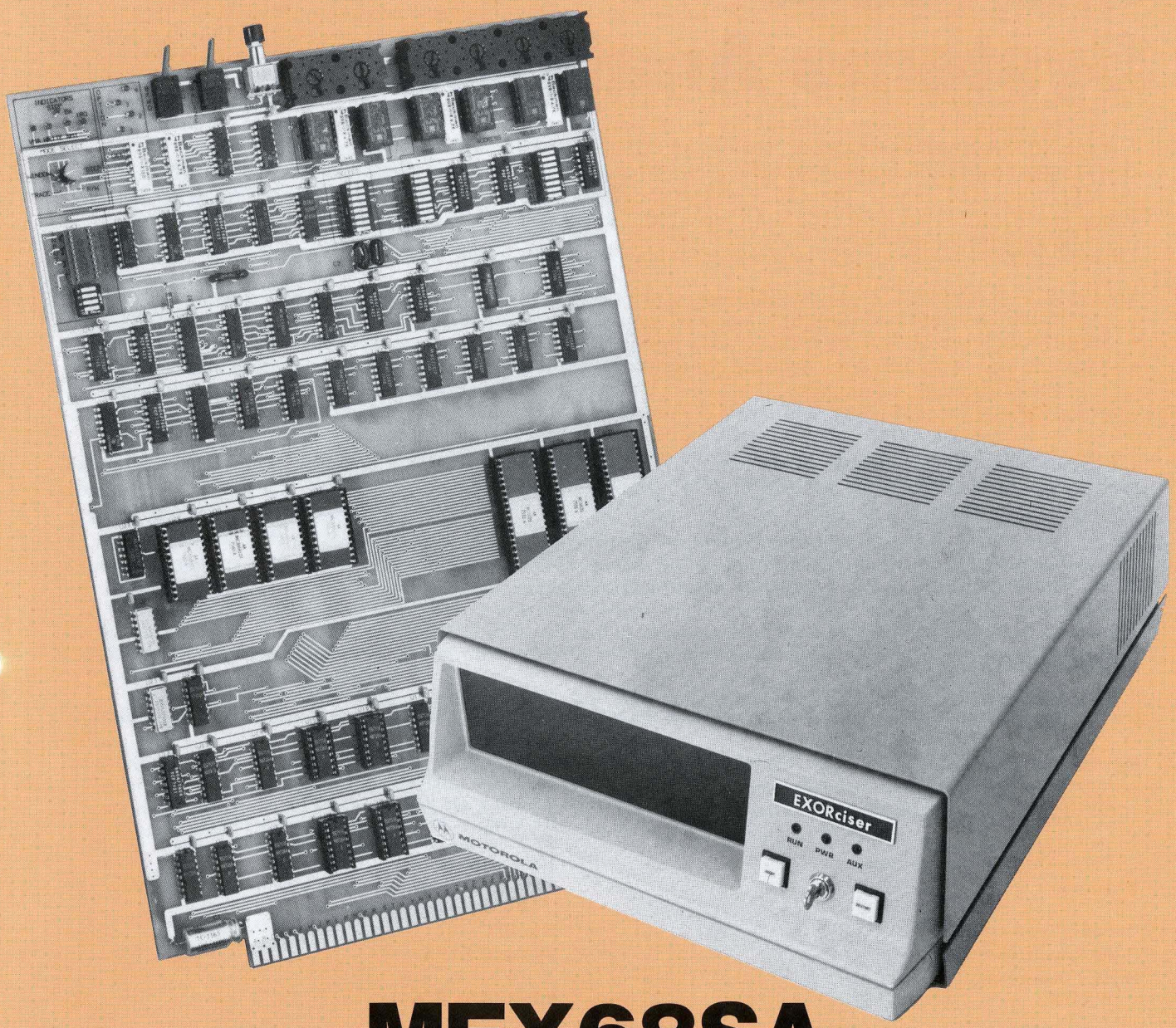


MEX68SA Systems Analyzer

For System Development and Troubleshooting

ISSUE A

MEX68SA Systems Analyzer

The MEX68SA Systems Analyzer provides an efficient and economical means of monitoring, analyzing, and troubleshooting M6800 Microprocessor Systems. This module connects directly into the MPU's bus and permits the user access to the operations being performed inside of his MPU. With a minor modification to the MPU's VMA signal, the Systems Analyzer is capable of performing the following functions:

- Stop the MC6800 MPU on detecting the selected compare conditions
- Step through the MPU's program
- Examine and, if required, change the contents in the MPU system's memory
- Trace through the MPU's program
- Monitor and record (takes a snapshot of) the MPU's operation during a selected portion of the MPU's program
- Print a hard copy of the data stored in the Systems Analyzer memory during the snapshot operation

The Systems Analyzer consists of six major blocks and has six modes of operation. The six major blocks are the Switch and Indicator Section, the Compare Section, the Memory Section, the Bus Buffer Section, the Hard Copy Interface Section, and the Control Section. The Control Section decodes the setting of the MODE SELECT switch and determines the module's mode of operation: MPU Run Mode, Step Mode, Standby Mode, Read/Write Mode, Trace Mode, and Window Mode. The module performs its snapshot operation in the Trace and Window Modes.

Specifications

(Note: Positive current flow is defined as flowing into the terminal, negative current flow as flowing from the terminal.)

Signal Characteristics	
Input Logic "0"	**0.0-0.85 V (-200 μA max at 0.4 V)**
Input Logic "1"	**2.0-5.25 V (25 μA max at 5.25 V)**
Output Logic "0"	**0.5 V max at 40 mA through a resistor to V_{CC}**
Output Logic "1"	**2.6 V min at -10 mA through a resistor to ground**
Output Off-State Leakage Current	**100 μA max at 2.6 V**
Memory Size	**128 x 32 bits of random access memory consisting of four MCM6810 RAM devices**
Operating Temperature	**0 to 70°C**
Power Requirements	**+5 Vdc @ 2.75 A**
Physical Dimensions	
W x H x T	**9.75 x 14.0 x 0.062 in.**

Systems Analyzer Circuitry

Switch and Indicator Section

This section provides the user with a means of entering the selected compare conditions and of monitoring the status of the MPU bus. The switch portion of this circuitry consists of four hexadecimal address switches, two hexadecimal data switches, and a connector to permit the user to insert up to four optional input signals that he wishes to monitor. The indicator portion of this circuit consists of four hexadecimal address displays, two hexadecimal data displays, and nine LED displays. The LEDs display the status of the MPU (running or halted), the status of the four MPU control signals (R/W, VMA, $\overline{IRQ}$, and $\overline{NMI}$), and the status of the four user-selected optional input signals to the module.

Compare Section

This section, when enabled, compares the MPU bus signals with the output of the hexadecimal switches in the switch and indicator section to detect the selected compare conditions. A switch in each of the compare lines can be enabled or disabled to meet the selected compare conditions. On detecting these conditions, this circuit applies a compare strobe to the other sections in the module.

Memory Section

This section consists of four MCM6810 128 x 8-bit RAM memory devices arranged into a 128 x 32-bit memory array. This memory, when enabled stores the bus status – 16 address lines, 8 data lines, VMA, R/W, $\overline{IRQ}$, $\overline{NMI}$, and the four user selected optional inputs – during each MPU $\phi 2$ clock pulse. The memory is enabled to record data during the snapshot operation in the Trace and Window Modes.

Bus Buffer Section

This section interfaces the Systems Analyzer Module into the EXORciser or the user's system. The data bus buffer devices may be changed to interface the module with a low-true or high-true system.

Hard Copy Interface Section

This section, working with the EXORciser's EXbug Firmware, permits the user to print a hard copy of the data stored in the module's memory. If the Systems Analyzer is not working with the EXORciser, and the user wishes to use the module's hard copy capability, he is required to develop the appropriate I/O routines in his system's program.

Control Section

This section decodes the setting of the MODE SELECT switch and determines which of the module's six modes of operation is to be used.

In the **MPU Run Mode** the Systems Analyzer is disabled and effectively removed from the user's system.

In the **Step Mode** the Systems Analyzer monitors the MPU bus and, on detecting the selected compare conditions, halts the MPU. The user now can step through the user's program.

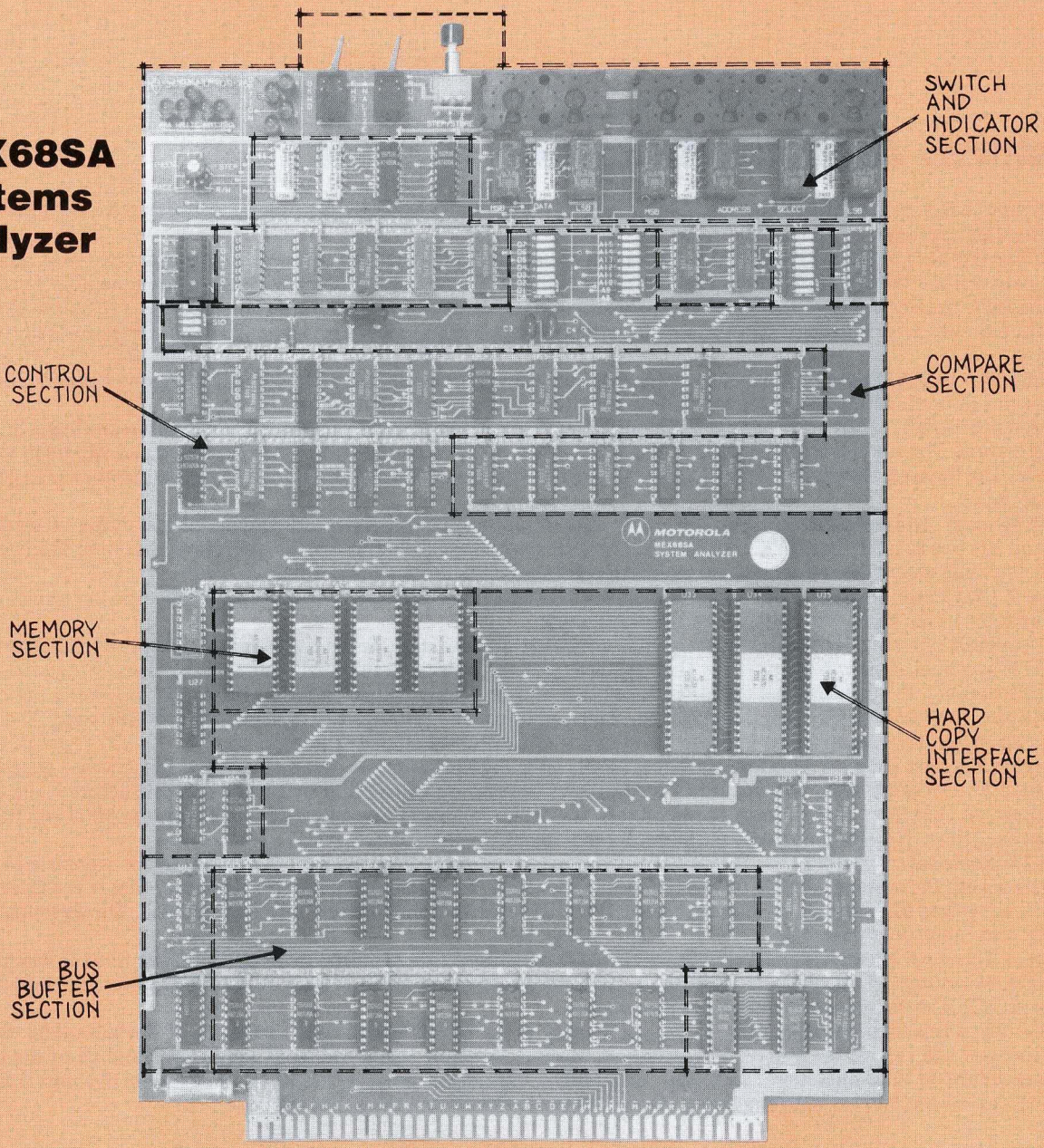
In the **Standby Mode** the Systems Analyzer holds the MPU in the state it was placed in while the module was in the Read/Write or Step Mode.

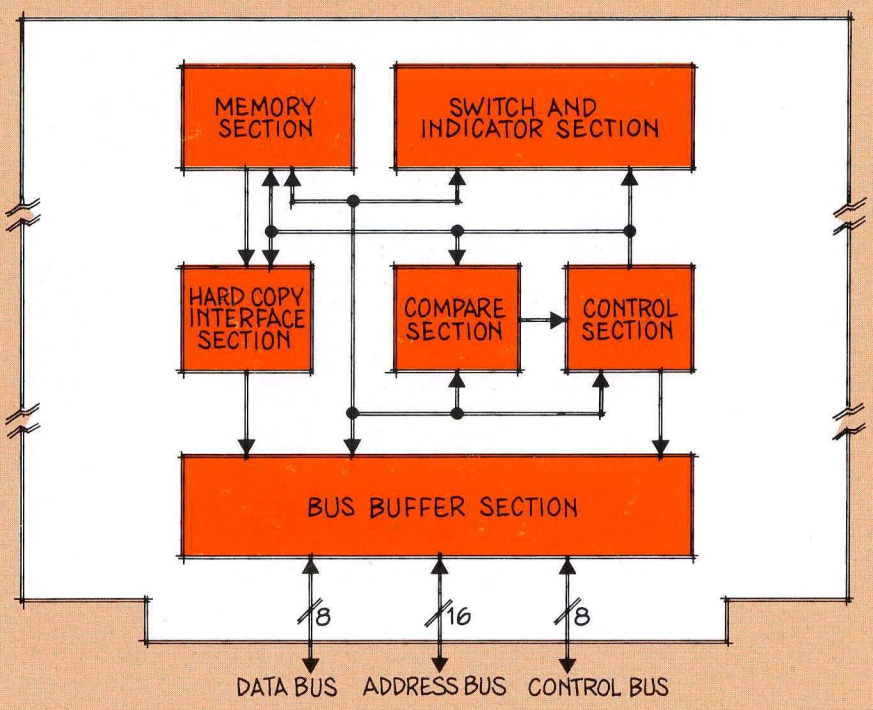
In the **Read/Write Mode** the Systems Analyzer halts the MPU on detecting the selected compare conditions. This module now permits the user to examine and, if required, change the contents in the MPU's memory. The hexadecimal switches in the Switch and Indicator Section select the memory location to be examined and the hexadecimal data switches select the data to be written into memory.

In the **Trace Mode** the Systems Analyzer stores the MPU bus status in its memory during each $\phi 2$ clock pulse. On detecting the selected compare conditions, the Systems Analyzer stores an additional 64 bus states and then halts the MPU. The user now can examine the 128 bus states – the 63 bus states before the selected compare conditions, the selected compare condition bus state, and 63 bus states after the selected compare conditions – recorded in the module's memory.

In the **Window Mode**, as in the Trace Mode, the Systems Analyzer stores the MPU bus states in its memory during each $\phi 2$ clock pulse. On detecting the selected compare conditions the module stores an additional 64 bus states and then stops storing data. In this mode, however, the MPU is not halted but continues running and the user has a snapshot or window view of the operations being performed in the selected portion of his program. The user can now examine the 128 bus states within the selected window area and, if desired, print a hard copy of these bus states.

MEX68SA Systems Analyzer





Systems Analyzer Interface Signals

The MEX68SA Systems Analyzer Module plugs directly into the EXORciser bus or may be connected to the MPU's bus in the user's system.

Data Bus (D0-D7) or Data Bus (D0-D7) – These eight bi-directional lines, when enabled, provide a two-way transfer of data between the MPU Module in the EXORciser or the MPU in the user's system and the selected memory location. When the MPU has been halted, the Systems Analyzer controls the flow of data on this bus. These bus signals in the EXORciser are low true. The user can, through installing the appropriate bus device, change these signals for high true operation.

Address Bus (A0-A15) – These 16 lines, when enabled, transfer the selected address to the system's memory and input/output devices. When the Systems Analyzer is halted, it controls this line.

Read/Write (R/W) – This MPU output signal indicates whether the MPU is performing a memory read (high) or write (low) operation. The normal standby state of this line is read. Also, when the MPU is halted, this signal will be in the read state. The Systems Analyzer, in halting the MPU, gains control of this signal and can initiate a memory read or write operation.

Valid Memory Address (VMA) – This line, when present, indicates to the memory and peripheral devices that the address on the bus is valid. The MPU's VMA output signal must be modified to allow the Systems Analyzer Module to pull this line high and address the memory and peripheral devices when the MPU is halted.

Phase 2 (ϕ2) Clock Signal – This signal is between 100 kHz and 1 MHz, and is used to synchronize the transfer of data on the data bus. This signal is controlled by the MPU clock.

Bus Available (BA) – This MPU output signal is normally in a low state. When activated, it will go high indicating that the MPU is available. This will occur if the Halt line is low or the MPU is in the WAIT state as the result of executing a WAIT instruction. At such time, all the MPU three-state output drivers will go to their off or high impedance state and all other outputs to their normally inactive state. An interrupt command removes the MPU from the WAIT state. The Systems Analyzer uses this signal to indicate the status of the MPU – halted or running.

Interrupt Request (IRQ) – This level sensitive input, on going low, requests that an interrupt sequence be generated in the system. The MC6800 MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At that time, if the interrupt mask bit in the MPU Condition Code Register is not set, the MPU will begin the interrupt sequence. The Systems Analyzer monitors this signal.

Non-Maskable Interrupt (NMI) – This level sensitive input, on going low, requests that an interrupt sequence be generated within the system. The MC6800 MPU will wait until it completes the current instruction that it is executing before it recognizes this request. At this time, the MPU will begin its non-maskable interrupt routine. The Systems Analyzer also monitors this signal.

Reset – This edge sensitive signal initiates an MC6800 MPU power-on vectored interrupt initialize routine when the user resets his systems. This signal, in addition to resetting the system's MPU, is used to reset and initialize the Systems Analyzer's MC6820 Peripheral Interface Adapter devices.

Halt – When this level sensitive signal is low, all activity in the MC6800 MPU will be halted. In the halt mode, the microprocessor will stop at the end of an instruction, the Bus Available signal will be at a high level, and all of the three-state lines will be in their high impedance state. The MPU's VMA signal must be modified to allow the Systems Analyzer Module access to the MPU system's memory and peripherals when it has halted the MPU.

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