



M6800B

Evaluation Module II

For Hardware Evaluation and Program Development

M6800B

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The M6800B Evaluation Module II is a Microcomputer that provides the user with an efficient and economical off-the-shelf means to evaluate the operating characteristics of the M6800 Microcomputer family of parts in various applications. It contains the following components:

- One M6800 Microprocessing Unit (MPU)
- Three MCM6810 128 x 8 Random Access Memories (RAM)
- One MCM6820 Peripheral Interface Adapter (PIA)
- One MCM6830 1024 x 8 Read Only Memory (ROM)
- Two MC6850 Asynchronous Communications Interface Adapters (ACIA)
- One MC14411 Bit Rate Generator (BRG)
- Data and address buffers

The M6800B Evaluation Module II interfaces with either a TTY (20 mA neutral current loop) or an RS-232C compatible terminal. This data terminal provides direct communication with the module's MINIBUG control program. The MINIBUG control program, stored in the module's read only memory, in conjunction with the selected data terminal, provides the following functions:

- Load data into the Evaluation Module
- Display and, if required, change the data in the module's random access memory
- Display and, if required, change the contents of the MPU registers
- Print out or punch (record) on tape the data stored in the module's memory
- Set the number of stop bits for data communication
- Run the user's program

The Evaluation Module provides the user with 256 bytes of random access memory on which to develop his programs. In addition, this module, through its address and data buffers, is capable of interfacing with additional memory and input/output modules.

The module's clock circuitry, in addition to generating the module's basic timing signals, provides the Evaluation Module with dynamic memory refresh capability on a cycle stealing basis and the ability to work with slow memories.

The MC14411 Bit Rate Generator provides the Evaluation Module with fourteen standard baud rates — six of which are jumper selectable. The MINIBUG II Firmware, in interfacing with the selected data terminal, is capable of transferring data at either 110 or 300 baud, dependent on the terminal.

The Evaluation Module also has the capability of connecting directly to a user's defined process or peripheral device through its MC6820 PIA and second MC6850 ACIA. The MC6820 PIA's dual input/output ports and control lines permit interfacing the Evaluation Module with keyboards, basic printers, displays, and similar devices. The MC6850 ACIA's serial communications port permits interfacing the Evaluation Module with modems, data terminals, and similar serial interface devices at one of the Bit Rate Generator's jumper selectable data transfer rates. Through the appropriate jumper connections, the Evaluation Module can be modified to operate at any one of 14 baud rates.

Options

Option	Part Number	Description
1	MEC6800B	Assembled and Tested Evaluation Module Assembly
2	MEC6800B1	Bareboard — Printed Circuit Board only. User supplies components.

Parts supplied with the MEC6800B — Three 16-pin component boards.
PIA Connector and Flatribbon Cable.
M6900B Evaluation Module II User's Guide.

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Specifications

Power Requirements	+5 Vdc @ 2 A +12 Vdc @ 50 mA -12 Vdc @ 50 mA
Clock Frequency	921.6 kHz
Signal Characteristics	
Connector P1	
Address Bus	Three-State TTL Voltage Compatible
Logic "0"	0.5 V max at 40 mA through a resistor to V _{CC}
Logic "1"	2.6 V min at -10 mA through a resistor to ground
Output Off-State Leakage Current	100 μ A max at 2.6 V
Data Bus	TTL Voltage Compatible
Input Logic "0"	0.0-0.85 V (-200 μ A max at 0.4 V)
Input Logic "1"	2.0-5.25 V (25 μ A max at 5.25 V)
Output Logic "0"	0.5 V max at 40 mA through a resistor to V _{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Control Bus	TTL Voltage Compatible
Input Logic "0"	TTL Voltage Compatible
Input Logic "1"	TTL Voltage Compatible
Output Logic "0"	0.5 V max at 40 mA through a resistor to V _{CC}
Output Logic "1"	2.6 V min at -10 mA through a resistor to ground
Connector P2, PIA Signals	
Data Signals	TTL Voltage Compatible
PA0-PA7 Input/Output Lines	Three-State TTL Voltage Compatible
PB0-PB7 Input/Output Lines	
Control Lines	TTL Voltage Compatible
CA1, CA2, and CB1	Three-State TTL Voltage Compatible
CB2	
Connector P3, Terminal Interface Signals	
Data Transfer Rate	110 or 300 Baud
Data Signal Characteristics	TTY (20 mA neutral current loop) or EIA RS-232C compatible
Reader Control Signal	Control signal for manual TTY devices modified for external control
Connector P4, Terminal Interface Signals	
Data Transfer Rate	110, 134.5, 300, 600, 1200 and 2400 Baud (with jumper modifications 75, 150, 200, 1800, 3600, 4800, 7200 and 9600).
Data Signals	EIA RS-232C compatible

Connections and Descriptions

Connector P1 — Data, Address, and Control Bus

Signal Mnemonic	Signal Name and Description
<u>IRQ</u>	<u>Interrupt Request</u> — This input signal requests that an interrupt sequence be generated within the MPU. The processor will wait until it completes the instruction that is being executed before it recognizes the request. Then, if the interrupt mask bit in the condition code register is not set (interrupt not masked), the MPU will begin an interrupt sequence. The MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur.
<u>NMI</u>	<u>Non-Maskable Interrupt</u> — This input signal requests that a non-maskable interrupt sequence be generated within the processor. The processor will complete the instruction that is being executed before it recognizes the <u>NMI</u> signal.
<u>VMA</u>	<u>Valid Memory Address</u> — This output indicates to the memory and peripheral devices that the address on the address bus is valid.
ϕ 2	<u>Phase 2 Clock signal</u> — This signal is derived from the memory clock and used to synchronize the transfer of data on the data bus.
<u>MEMCLK</u>	<u>Memory Clock</u> — This is the basic 921.6 kHz clock signal used by the Evaluation Module to generate its ϕ 1 and ϕ 2 clock signals. A dynamic memory device would use this signal to control its timing.

Connections and Descriptions

Connector P1 — Data, Address, and Control Bus (continued)

Signal Mnemonic	Signal Name and Description
TSC	Three-State Control — This input, when high, causes all of the address lines and read/write line to go to their off, or high-impedance, state. The valid memory address, valid user's address, and the bus available signals will be forced low. The data bus is not affected by the three-state control.
BA	Bus Available — This output signal will normally be a low level. When activated, it will go high indicating that the address bus is available. This will occur if the <u>Halt</u> line is low or the MPU is in the WAIT state as the result of executing a WAIT instruction.
MEMRDY	Memory Ready — This signal enables the Evaluation Module to work with slow memories. The Evaluation Module, on receiving a low level Memory Ready input, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 2$ high.
<u>D0-D7</u>	Data Bus — These bi-directional lines, when enabled, transfer data between the MPU and any external modules.
<u>A0-A15</u>	Address Bus — This address line, when enabled transfers the MPU program counter output to any external modules.
<u>HALT</u>	<u>Halt</u> — When this input is in the high state, the MPU will fetch the instruction addressed by the program counter and start execution. When low all activity in the MPU will be halted.
<u>RESET</u>	<u>Reset</u> — This line goes low when the RESET switch is actuated and may be used to reset any external devices. The RESET switch, on being actuated, initiates a MC6800 MPU cold-start vectored interrupt routine.
<u>R/W</u>	<u>Read/Write</u> — This MPU output signal indicates to the external modules whether the MPU is in a read (high) or a write (low) state. The normal standby state of this signal is read (high).
<u>REFREQ</u>	<u>Refresh Request</u> — This signal, when present, initiates a memory refresh operation. The Evaluation Module, on receiving this input from an external module, stops generating the $\phi 1$ and $\phi 2$ clock signals with $\phi 1$ high and, through the Refresh Grant command, instructs the dynamic memory modules to refresh their memories.
<u>REFGNT</u>	<u>Refresh Grant</u> — This signal instructs the dynamic memory modules to refresh their memories.
<u>VUA</u>	<u>Valid User's Address</u> — This signal indicates to the memory and peripheral devices that the address on the bus is valid. On Evaluation Module II, VUA is the same signal as VMA.

Connector P2 — Peripheral Interface Adapter Signals

Evaluation Module II provides the user with the capability of connecting a parallel peripheral device to the module's MC6820 PIA. This PIA has dual 8-bit input/output ports — PA0-PA7 and PB0-PB7 — along with four control lines — CA1, CA2, CB1, and CB2. Refer to the M6800 System Design Data for details on these signals.

Connector P3 — TTY/RS-232C Terminal Interconnection Signals

TTY IN	Serial Data In — This line accepts the input from a TTY terminal.
TTY OUT	Serial Data Out — This line transfers data to a TTY terminal.
—	Reader Control — This signal provides the control required to operate the paper tape reader on a modified manual TTY data terminal. The terminal now is under MPU control.
—	Serial Data Common — This line provides a return for the Serial Data In and Serial Data Out signals.
—	Reader Common — This line is connected to Evaluation Module II ground and provides a return for the Reader Control signal.
RS-232 IN	RS-232C Input — This line accepts the data input from a terminal.
RS-232 OUT	RS-232 Output — This line transfers data to a terminal.
DCD	Data Carrier Detect — This high impedance TTL input, when high, inhibits and initializes the receiver section of the MC6850 ACIA.
RTS	Request to Send — This line, when used with an RS-232C terminal, informs the terminal that Evaluation Module is ready to receive data.
CTS	Clear To Send — This line is a low level when an RS-232C terminal is connected to Evaluation Module II and informs the terminal to transfer data.

Connector P4 — Asynchronous Device Signals

Evaluation Module II, through the other MC6850 ACIA device, provides the user with the capability of connecting asynchronous communications devices to the module. The user can interface directly with the module's ACIA or through the module's RS-232C level converters. The RS-232C interconnection signals are described above. Refer to the M6800 System Design Data for details on the ACIA's signals.

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