MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6843

FLOPPY DISK CONTROLLER (FDC)

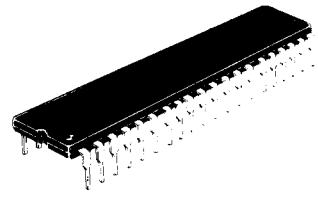
The MC6843 Floppy Disk Controller performs the complex MPU/Floppy interface function. The FDC was designed to optimize the balance between Hardware and Software in order to achieve integration of all key functions and maintain flexibility.

The FDC can interface a wide range of drives with a minimum of external hardware. Multiple drives can be controlled with the addition of external multiplexing rather than additional FDCs.

- Format Compatible with IBM 3740
- User Programmable Read/Write Format
- Ten Powerful Macro Commands
- Macro-End Interrupt Allows Parallel Processing of MPU and FDC
- Controls Multiple Floppies with External Multiplexing
- Direct Interface with M6800 Bus
- Programmable Step and Settling Times Enable Operation with a Wide Range of Floppy Drives
- Offers Both Program Controlled I/O (PCIO) and DMA Data Transfer Mode
- Free-Format Read or Write
- Single 5-Volt Power Supply
- All Registers Directly Accessible

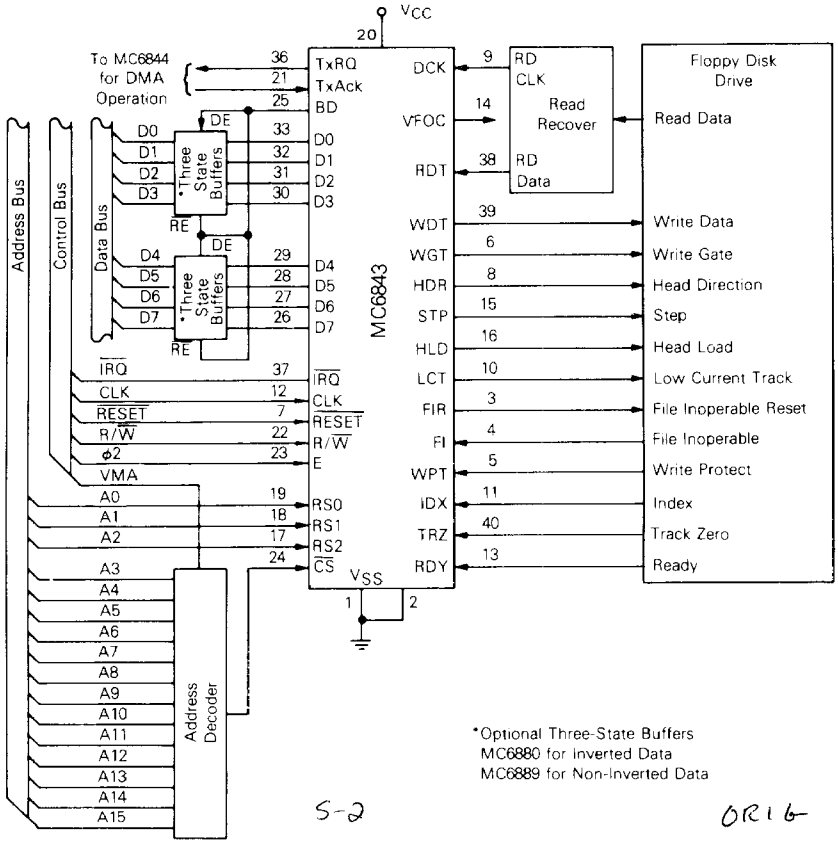
MOS
(N-CHANNEL, SILICON-GATE)

FLOPPY DISK CONTROLLER



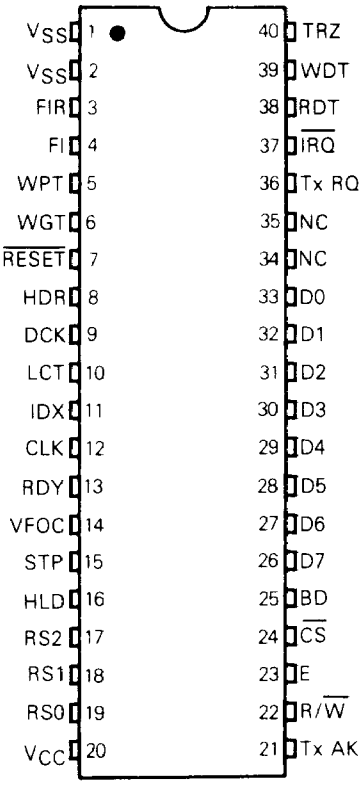
P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 — SYSTEM BLOCK DIAGRAM



*Optional Three-State Buffers
MC6880 for Inverted Data
MC6889 for Non-Inverted Data

FIGURE 2 — PIN ASSIGNMENT



DS9837
(Replaces ADI-477)

MAXIMUM RATING

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance	θ_{JA}	100	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

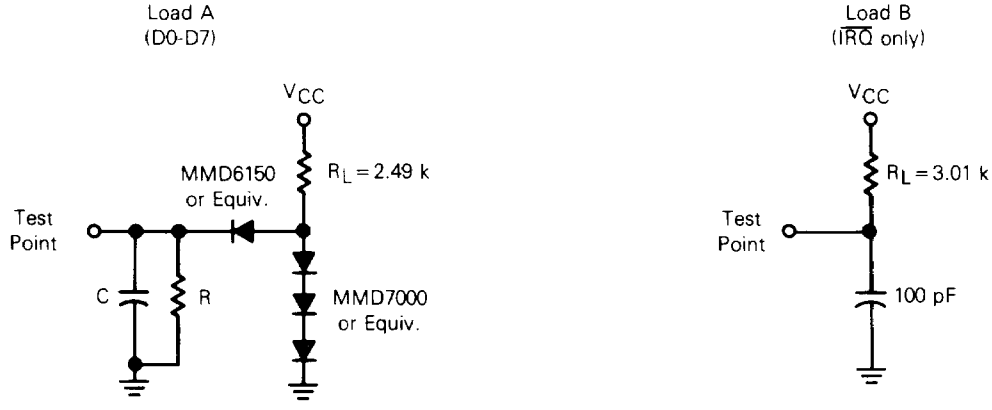
$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

FIGURE 3 — TEST LOADS



C = 130 pF for D0-D7
= 30 pF for HLD, STP, HDR, LCT, WGT, FIR TxRQ, BD
R = 11.7 k for D0-D7
= 24 k for HLD, STP, HDR, LCR, LCT, WGT, FIR TxRQ, BD

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	V
Input Low Voltage		V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	V
Input Leakage Current (V_{in} = 0 to 5.5 V)		I_{in}	–	1.0	2.5	μA
Three-State Input Leakage Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.5 V)	D0-D7	I_{IZ}	– 10	2.0	10	μA
Output High Voltage (I_{load} = – 205 μA) (I_{load} = – 100 μA)	D0-D7 Other Outputs	V_{OH}	V_{SS} + 2.4 V_{SS} + 2.4	– –	– –	V
Output Low Voltage (I_{load} = 1.6 mA)		V_{OL}	–	–	V_{SS} + 0.4	V
Three-State Output Leakage Current (V_{OH} = 2.4 V)	IRQ	I_{OZ}	–	1.0	10	μA
Internal Power Dissipation (Measured at $T_A = T_L$ to T_H)		P_{INT}	–	–	750	mW
Input Capacitance (V_{in} = 0 V, f = 1.0 MHz, T_A = 25°C)	Enable D0-D7 All Others	C_{in}	– – –	– – –	10 12.5 10	pF
Output Capacitance (V_{in} = 0 V, f = 1.0 MHz, T_A = 25°C)	All Outputs	C_{out}	–	–	10	pF
Clock Pulse Width, Low (CLK)		PW_{CL}	400	–	–	ns
Clock Pulse Width, High (CLK)		PW_{CH}	400	–	–	ns
Master Clock Period (CLK)		t_{MC}	1.0	–	–	μs
Data Clock Pulse Width, Low (DCK)		PW_{DL}	1.3	1.95	–	μs
Data Clock Pulse Width, High (DCK)		PW_{DH}	1.3	1.95	–	μs
Data Clock Period (DCK)		t_{DC}	2.5	4.0	–	μs
Read Data to Data Clock Delay Time 1		t_{RDD1}	0.55	1.0	–	μs
Read Data to Data Clock Delay Time 2		t_{RDD2}	0.55	1.0	–	μs
Read Data Pulse Width, High		t_{RDH}	–	1.0	–	μs
Read Data Pulse Width, Low		t_{RDL}	–	1.0	–	μs
Index Pulse Width, High		PW_{IDX}	1.0	–	–	μs
Transfer Request Release Time		t_{TR}	–	–	450	ns
Interrupt Request Release Time		t_{IR}	–	–	1.2	μs
Bus Direction Delay Time		t_{DBD}	–	–	330	ns
Write Data Pulse Width, High (f_C = 1.0 MHz)		PW_{WD}	–	1.0	–	μs
Write Data Cycle Time (f_C = 1.0 MHz)		t_{cycWD}	–	2.0	–	μs
Step Pulse Width, High (f_C = 1.0 MHz)		PW_{STP}	–	32	–	μs
Step Cycle Time* (f_C = 1.0 MHz)		t_{cycSTP}	1.0	–	15	ms
Write Gate to Write Data Delay (SSW, SWD, MSW)		t_{GD1}	0.7	1.0	1.3	μs
Write Gate Hold Time		t_{GH}	0	–	0.3	μs
Write Gate to Write Data Delay (FFW)		t_{GD2}	0.2	–	2.0	μs
CLK to $\overline{IRQ}$ Delay		t_{IRQC}	–	–	1.2	μs
CLK TO ISR0-3 Delay		t_{ISRD}	–	–	0.7	μs
Index Pulse to STRB Bit 3 Delay		t_{IRQI}	–	–	1.8	μs
Index Pulse to $\overline{IRQ}$ Delay		t_{STRB3}	–	–	1.0	μs
Data Clock to Transfer Request Delay		t_{DTx}	400	–	700	ns
Signal Rise and Fall Times		t_r, t_f	–	–	25	ns

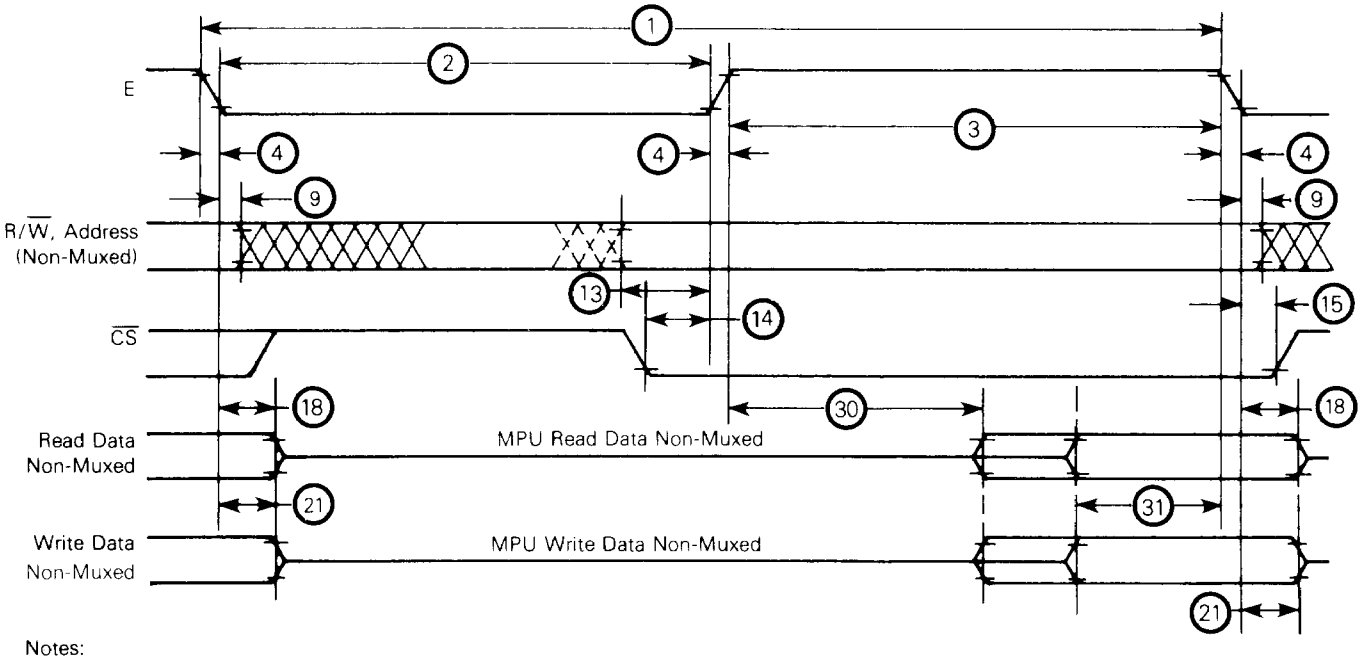
*Step (STP) cycle time is programmable.

BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

Ident. Number	Characteristic	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	1.0	10	μs
2	Pulse Width, E Low	PW_{EL}	430	9500	ns
3	Pulse Width, E High	PW_{EH}	450	9500	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	ns
9	Non-Muxed Address Hold Time	t_{AH}	10	–	ns
13	Address Setup Time Before E	t_{AS}	80	–	ns
14	Chip-Select Setup Time Before E	t_{CS}	80	–	ns
15	Chip-Select Hold Time	t_{CSH}	10	–	ns
18	Peripheral Read Data Hold Time Provided	t_{DHR}	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	ns
30	Peripheral Output Data Delay Time	t_{DDR}	–	290	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	–	ns

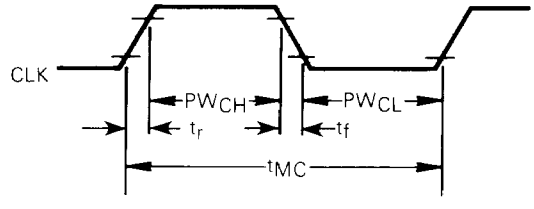
*The data bus output buffers are no longer sourcing or sinking current by t_{DHR}max (High Impedance).

FIGURE 4 – BUS TIMING CHARACTERISTICS (See Notes 1 and 2)



Notes:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 5 – MASTER CLOCK (CLK)



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 6 — READ DATA TIMING

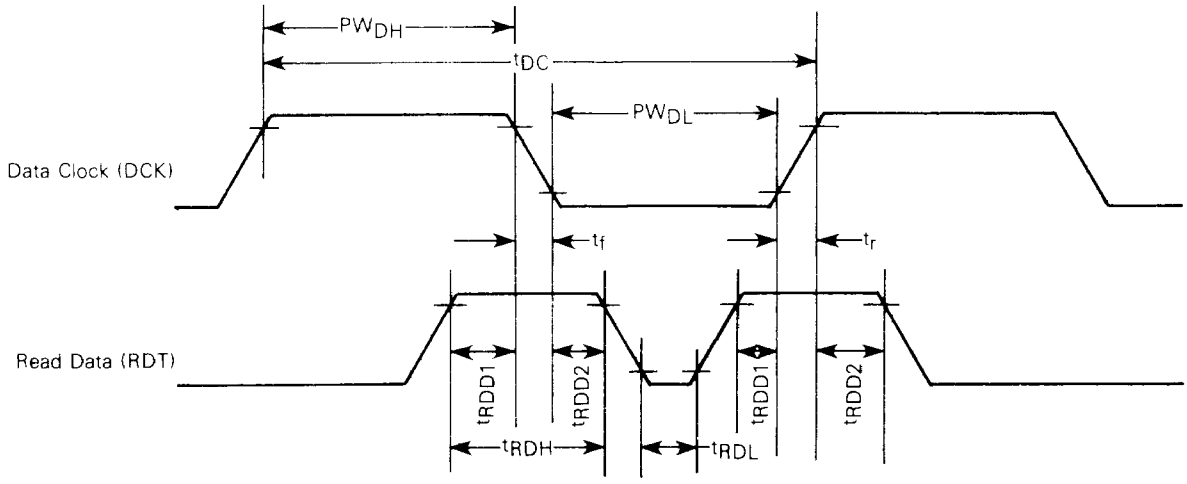


FIGURE 7 — INDEX TIMING

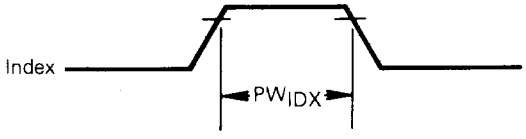


FIGURE 8 — $\overline{IRQ}$ RELEASE TIME

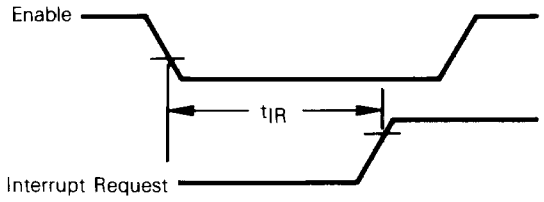


FIGURE 9 — DATA BUS DIRECTION TIMING

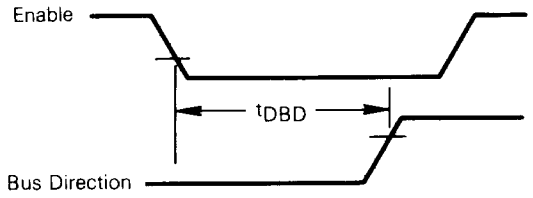
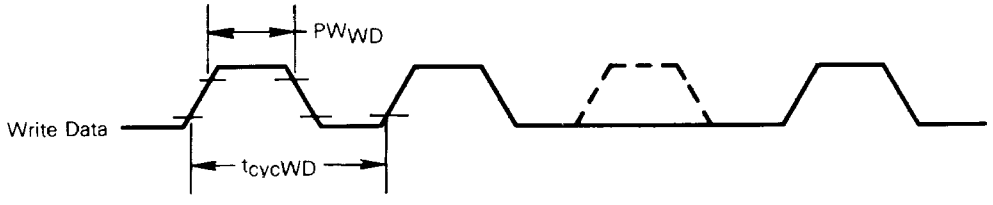


FIGURE 10 — WRITE DATA TIMING



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 11 — STEP TIMING (PROGRAMMABLE)

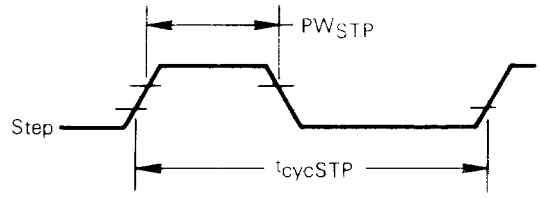


FIGURE 12 — TxRQ RELEASE TIMING

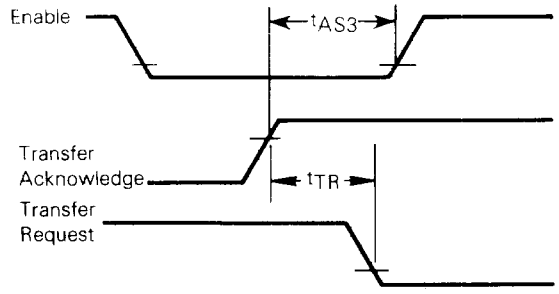


FIGURE 13 — DELAY TIME FROM DATA CLOCK TO TRANSFER REQUEST (t_{DTx})

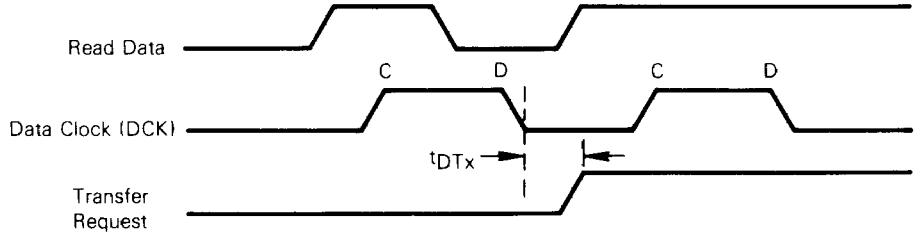
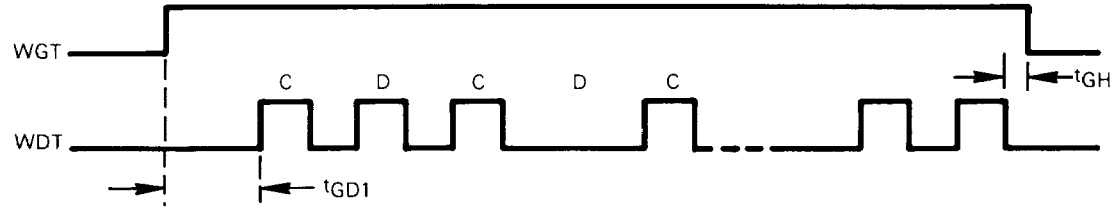


FIGURE 14 — WRITE DATA versus WRITE GATE TIMING

a — SSW, SWD and MSW commands (Single Sector Write, Single Sector Write with Deleted Address Mark, and Multiple Sector Write)



b — FFW Command (Free Format Write)

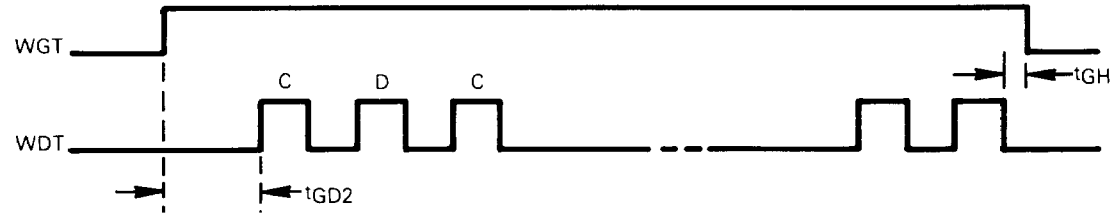
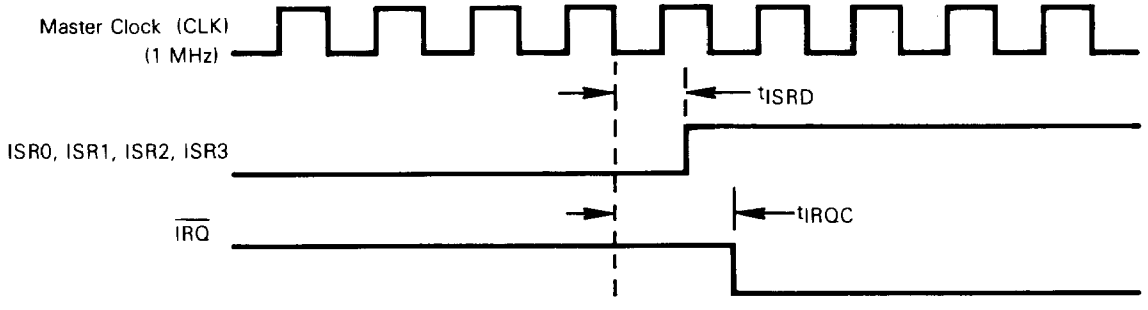
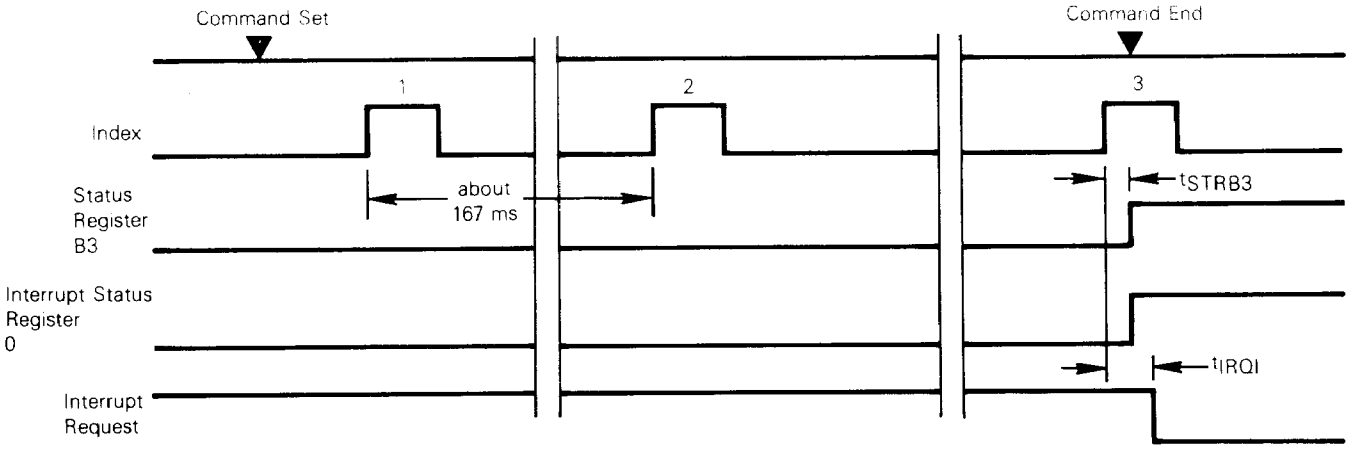


FIGURE 15 — INTERRUPT STATUS REGISTER AND INTERRUPT REQUEST TIMING



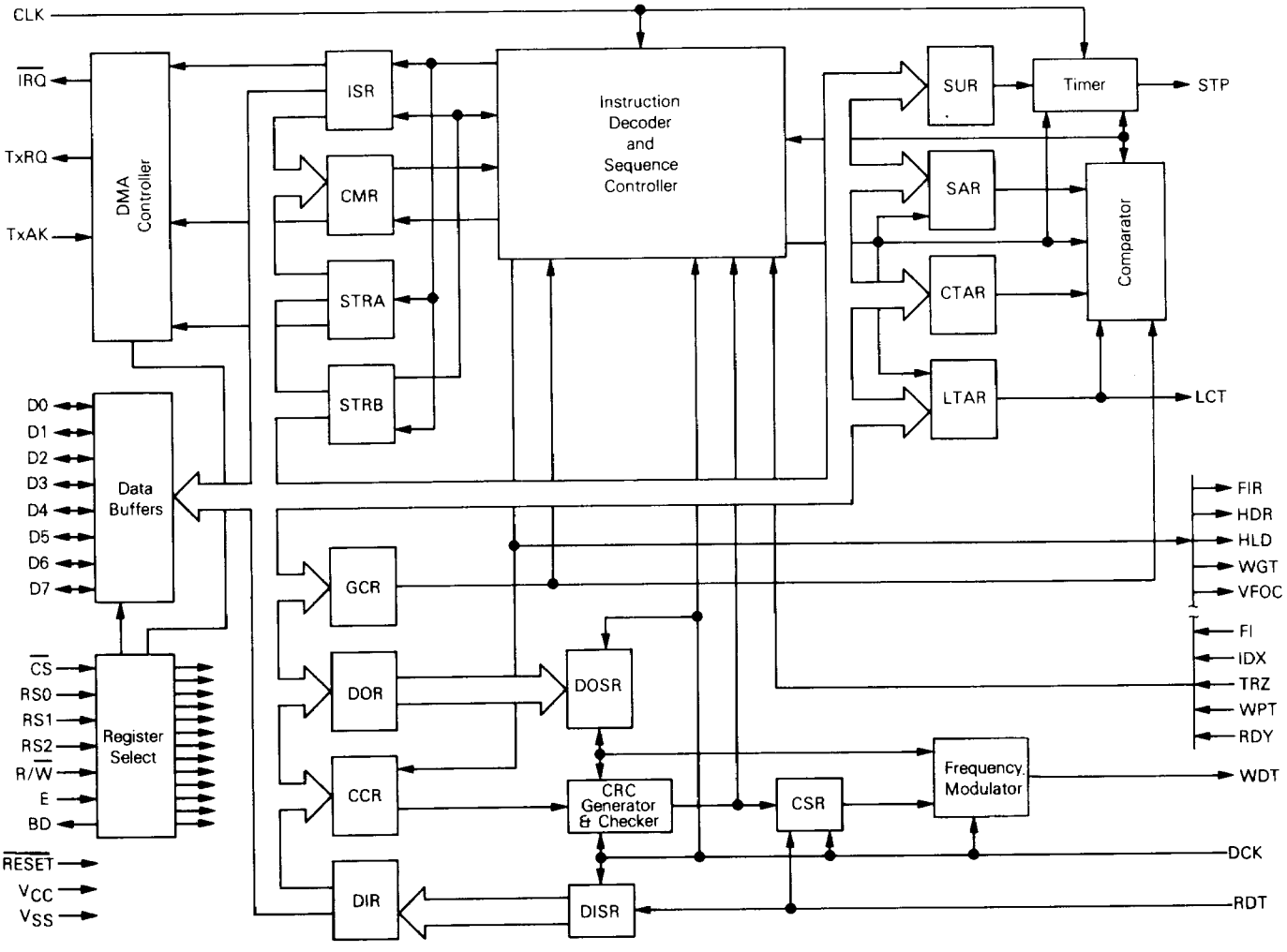
Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 16 — TRACK NOT EQUAL ERROR TIMING



Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 17 — INTERNAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The MC6843 FDC is a single-density controller which is IBM compatible. Data from the drive is clocked into the FDC by an external phase lock loop oscillator. Internal synchronization to the data stream is handled automatically. A 1 MHz clock is used as a timing signal for the internal functions of the FDC, such as head load and step, as well as shifting data serially to the drive. Status bits are provided to indicate various error conditions and status of the drive. DMA or polled I/O modes are available.

Register Section

The register section consists of twelve user-accessible registers used for controlling a floppy disk drive. All twelve are connected by the internal data bus to allow the processor access to them.

Data Output Register (DOR) — The DOR is an 8-bit register which holds the data to be written onto the disk. The information is stored here by the bus interface.

Data Input Register (DIR) — The data words read from the disk are stored in the 8-bit DIR until read by the bus interface.

Current-Track Address Register (CTAR) — CTAR is a 7-bit register containing the address of the track over which the R/W head is currently positioned.

Command Register (CMR) — The macro commands are written to the 8-bit CMR to begin their execution.

Interrupt Status Register (ISR) — The four bits of the ISR represent the four conditions that can cause an interrupt to occur.

Set-Up Register (SUR) — Variable Seek and Settling times are programmed by the SUR. Four bits are used to program the track-to-track seek time and four bits are used to program the head settling time for the floppy disk drive used with the FDC.

Status Register A (STRA) — The eight bits of STRA are used to indicate the state of the floppy disk interface.

Sector Address Register (SAR) — SAR contains the 5-bit sector address associated with the current data transfer.

Status Register B (STRB) — The eight error flags of STRB are used to signify error conditions detected by the FDC or generated by the floppy disk drive.

General Count Register (GCR) — The seven bits of GCR contain the destination track address when a SEK (seek) macro command is being executed. If a multi-sector Read or Write macro command is being executed, GCR contains the number of sectors to be read or written.

CRC Control Register (CCR) — The two bits of the CCR are used to enable the CRC and shift the CRC for the Free-Format Commands.

Logical-Track Address Register (LTAR) — The 7-bit track address used for read and write operations is stored in the LTAR by the bus interface.

Serializing Section

The serializing section handles the serial-to-parallel and parallel-to-serial conversions for Read/Write operations, as well as CRC generation/checking and the generation/detection of the clock pattern. The Data Output Shift Register (DOSR), Data Input Shift Register (DISR), CRC Generator/Checker, and Clock Shift Register (CSR) comprise the serializing section of the FDC.

Bus Interface

The Bus Interface section provides the timing and control logic that allows the FDC to operate with the M6800 bus, and is comprised of the Data Buffers, DMA Control, and the Register Select circuitry.

Control

The internal timing and control signals which sequence the FDC are derived from the macro instructions by the control section.

PIN DESCRIPTION

POWER PINS

V_{CC}: Input

+5 volt (±5%) power input.

V_{SS}: Input

Power Supply Ground.

BUS PINS

Reset Input — The $\overline{RESET}$ input is used to initialize the FDC. When $\overline{RESET}$ becomes Low, the state of the outputs is defined by the table below:

Output	State of Output	Output	State of Output
FIR	Low	HLD	Low
WGT	Low	TxRQ	Low
HDR	Low	IRQ	High
STP	Low	WDT	Low

Registers which are affected by $\overline{RESET}$ are shown in Table 7.

Interrupt Request ($\overline{IRQ}$) Output — The $\overline{IRQ}$ line is an open-drain output that becomes a low level when the FDC requests an interrupt. Interrupt requests are controlled by the interrupt enables in CMR (Command Register) with the function causing the interrupt shown in ISR (Interrupt Status Register).

Data Bus 0-Data Bus 7 (D0-D7) Bidirectional — The eight bidirectional data lines allow the transfer of data between the FDC and the controlling system. The output buffers are three-state drivers that are enabled when the FDC is transferring data to the data bus.

Enable (E) Input – The E input to the FDC causes data transfers to occur between the FDC and the system controlling the FDC (MC6800 MPU, DMA Controller, etc.) E must be a logic '1' (high level) for any transfer to be enabled on D0-D7. The E input is normally connected to system $\phi 2$.

Chip-Select (CS) Input – The $\overline{CS}$ input, in conjunction with the E input, is used to enable data transfers on D0-D7. E must be a high level and $\overline{CS}$ must be a low level to enable the transfer. The TxAK input being a high level (logic '1') performs a function similar to $\overline{CS}$ being a low level.

Read/Write (R/$\overline{W}$) Input – The R/$\overline{W}$ input is issued by the system controlling the FDC (MC6800 MPU, DMA Controller, etc.) to signify if a read or write operation is to be performed on the FDC. When TxAK is a low level, R/$\overline{W}$ is used in conjunction with $\overline{CS}$ and RS0-RS2 to determine which register is accessed by the bus as shown in Table 1. When TxAK is a high level, R/$\overline{W}$ is used to select either the DOR or DIR to the data bus (see description of TxAK input).

Register Select 0-Register Select 2 (RS0-RS2) Input – RS0-RS2, in conjunction with the R/$\overline{W}$ input, are used to select one of the user accessible registers in the FDC as shown in Table 1.

TABLE 1 – ADDRESS CODES FOR USER ACCESSIBLE REGISTERS

TxAK	RS2	RS1	RS0	R/$\overline{W}$	Registers
0	0	0	0	0	DOR (Data Out Register)
				1	DIR (Data In Register)
0	0	0	1	1/0	CTAR (Current Track Address Register)
0	0	1	0	0	CMR (Command Register)
				1	ISR (Interrupt Status Register)
0	0	1	1	0	SUR (Set Up Register)
				1	STRA (Status Register A)
0	1	0	0	0	SAR (Sector Address Register)
				1	STRB (Status Register B)
0	1	0	1	0	GCR (General Count Register)
0	1	1	0	0	CCR (CRC Control Register)
0	1	1	1	0	LTAR (Logical Track Address Register)

Transfer Request (TxRQ) Output – TxRQ is used in the DMA mode to request a data transfer by the DMAC. TxRQ is a high level if the FDC is in the DMA mode (CMR bit 5 is set) when a data transfer request occurs (STRA bit 1 is set). It is reset to a low level (logic '0') when TxAK becomes a high level (logic '1'). Data transfer errors will occur if TxAK does not reset TxRQ before the next data transfer is required.

Transfer Acknowledge (TxAK) Input – TxAK is generated by the system controlling the FDC (MC6800 MPU, DMA Controller, etc.) and is a response to a TxRQ issued by the FDC. A high level (logic '1') on TxAK causes the FDC to neglect the state of RS0-RS2 and $\overline{CS}$ causing the FDC to select the DOR (Data Output Register) or DIR (Data Input Register) to the data bus (D0-D7) as shown in Table 2.

TABLE 2 – REGISTER SELECTION FOR DMA TRANSFERS

TxAK	RS0-RS2	$\overline{CS}$	R/$\overline{W}$	Register Selected
1	X	X	1	DOR
1	X	X	0	DIR

This mode of operation is normally used for DMA (Direct Memory Access) transfer with the FDC.

When TxAK is a low level the registers are selected by $\overline{CS}$, R/$\overline{W}$ and RS0-RS2 as shown in Table 1.

Bus Direction (BD) Output – The BD output is provided to control bidirectional buffers on the data bus (D0-D7) as shown in Figure 1. Its polarity is shown by Table 3.

TABLE 3 – BUS DIRECTION (BD) STATES

TxAK	$\overline{CS}$	BD
1	X	R/$\overline{W}$
0	1	0
0	0	R/$\overline{W}$

(Operation of BD, as defined by this chart, allows the FDC to function with the DMA Controller MC6844).

I/O AND CONTROL PINS

Master Clock (CLK) Input – The CLK input is used to generate various timing sequences internal to the FDC. The head settling and seek time, as well as the data and data clock timing, are generated from the CLK input signal.

Head Load (HLD) Output – HLD is used to notify the disk drive that the R/W head should be loaded (placed in contact with the media). When the FDC is ready for the head to load, HLD is a high level (logic '1'). A low level (logic '0') on HLD indicates the head should be unloaded.

Step (STP) Output – The STP output, in conjunction with HDR, is used to control head movement. A 32 μs wide positive (logic '1') pulse is generated on STP, to move the R/W head one track in the direction defined by the HDR output. The period of the STP signal is programmable by the SUR (Set-Up Register). The number of pulses generated on STP is the difference between the contents of the CTAR (Current Track Address Register) and the GCR (General Count Register) which contains the track address to which the head is to be moved.

Head Direction (HDR) Output – The HDR signal controls the direction of head movement. A high level (logic '1') signifies the head should step to the inside (toward the hub) of the disk. A low level (logic '0') indicates the direction of head movement should be to the outside of the disk.

Low-Current Track (LCT) Output – The LCT signal is used to control the level of write current used by the disk drive. LCT is a low level (logic '0') when the write head is positioned over tracks 0-43. If it is over tracks 44-76, LCT is a high level (logic '1'). LCT is determined from the contents of the Current Track Address Register (CTAR).

Write Gate (WGT) Output – When a write operation is being performed, WGT is a logic '1' (high level). For a read operation, WGT is a low level (logic '0').

File-Inoperable Reset (FIR) Output – FIR is an output from the FDC to the floppy disk drive to reset it from an inoperable status. If the FI input is a '1', a 1 μs pulse is generated on the FIR output whenever Status Register B is read.

File Inoperable (FI) Input – FI is an input to the FDC from the drive. A high level indicates the drive is in an inoperable state. Its current state can be examined by reading bit 5 of Status Register B (STRB).

Track Zero (TRZ) Input – The TRZ input is reflected by bit 3 of STRA (Status Register A). The TRZ input must be a high level (logic '1') when the R/W head of the drive is positioned over track zero. A logic '1' on this input inhibits step pulses during a Seek Track Zero command.

Index (IDX) Input – The index input is received from the floppy disk drive and is used to sense the index hold in the disk media. The IDX signal is used to initialize the internal FDC timing. The state of the IDX input is reflected by bit 6 of Status Register A (STRA). A high level (logic '1') is to indicate the index hole is under the index sensor. The index input is used to count the number of disk revolutions while searching for the address ID field (see description of STRB bit 3).

Ready (RDY) Input – The ready input is received from the disk drive and can be read as bit 2 of STRA (Status Register A). A high level (logic '1') indicates the drive is ready and allows the FDC to operate the drive.

Write Protect (WPT) Input – WPT is an input indicating when the media is Write Protected. A high level during an FDC write operation results in a Write Error (STRB bit 6) but the FDC continues to perform the write function. The state of the WPT input can be read by examining bit 4 of the Status Register A (STRA).

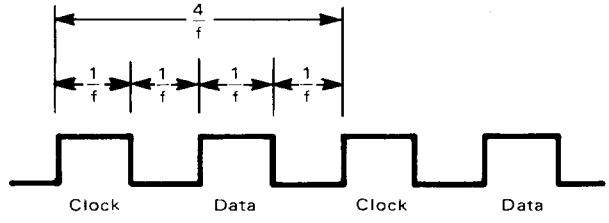
DATA PINS

Data Clock (DCK) Input – Data from the drive is clocked into the FDC on both positive and negative edges of the DCK input. This signal is generated from the Read Recovery Circuit.

Read-Data (RDT) Input – RDT is the serial data input from the Read Recovery Circuit. The data stream includes both the clock and the data bits and must be presynchronized to the Data Clock (DCK).

Write-Data (WDT) Output – WDT is the double frequency modulated data output from the FDC. The time between clock bits is 4/f where f is the frequency of the CLK input. The pulse width for both clock and data is 1/f (see Figure 18). For the normal CLK frequency of 1 MHz the write period is 4 μs, the clock pulse width is 1 μs and the data pulse width is 1 μs. Figure 18 shows the relationship between the WDT output and the frequency of the CLK inputs.

FIGURE 18 – WDT OUTPUT TIMING



f = Frequency of the CLK Input. To insure IBM3740 compatibility the clock frequency must be 1 MHz.

Variable-Frequency Oscillator Control (VFOC) Output – VFOC is used as a sync signal during system diagnostics. Waveforms are shown in Figure 19.

FORMAT

The format used by the MC6843, shown in Figure 20, is compatible with the soft sector format of the IBM 3740.

FIGURE 19 – VARIABLE FREQUENCY OSCILLATOR CONTROL WAVEFORM
(Relation Between WGT and VFOC)

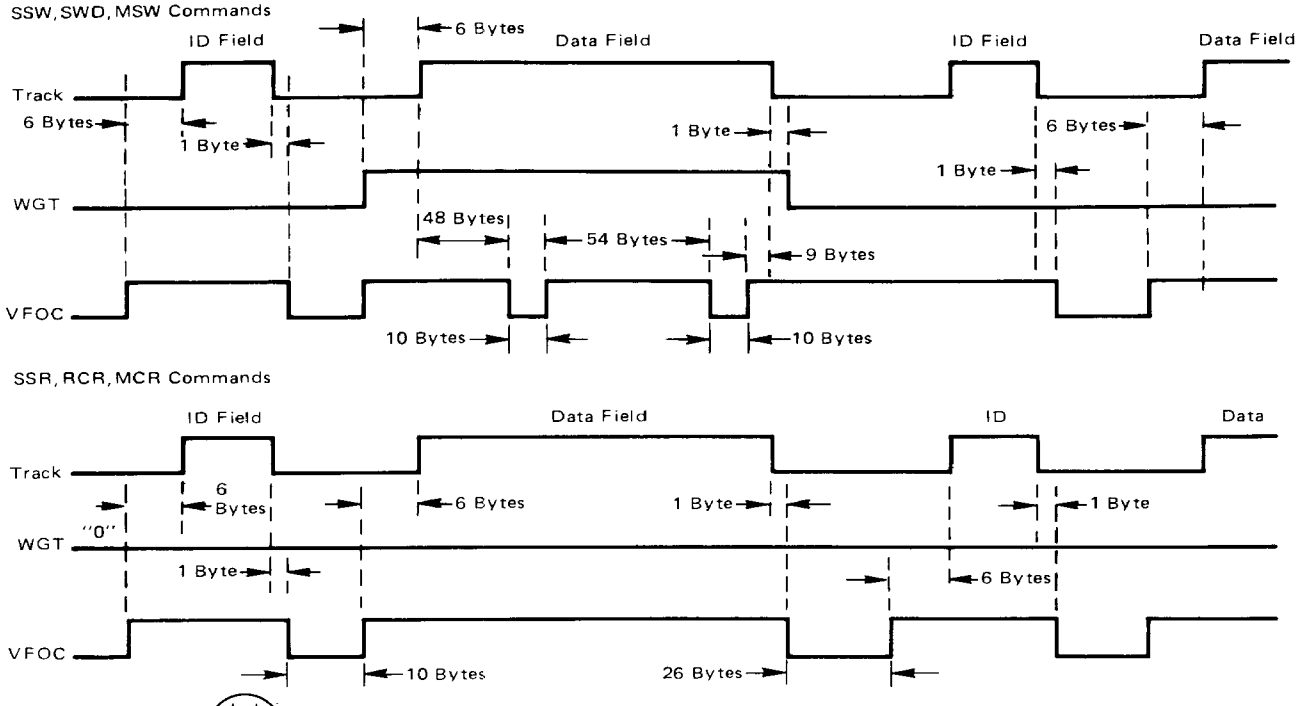
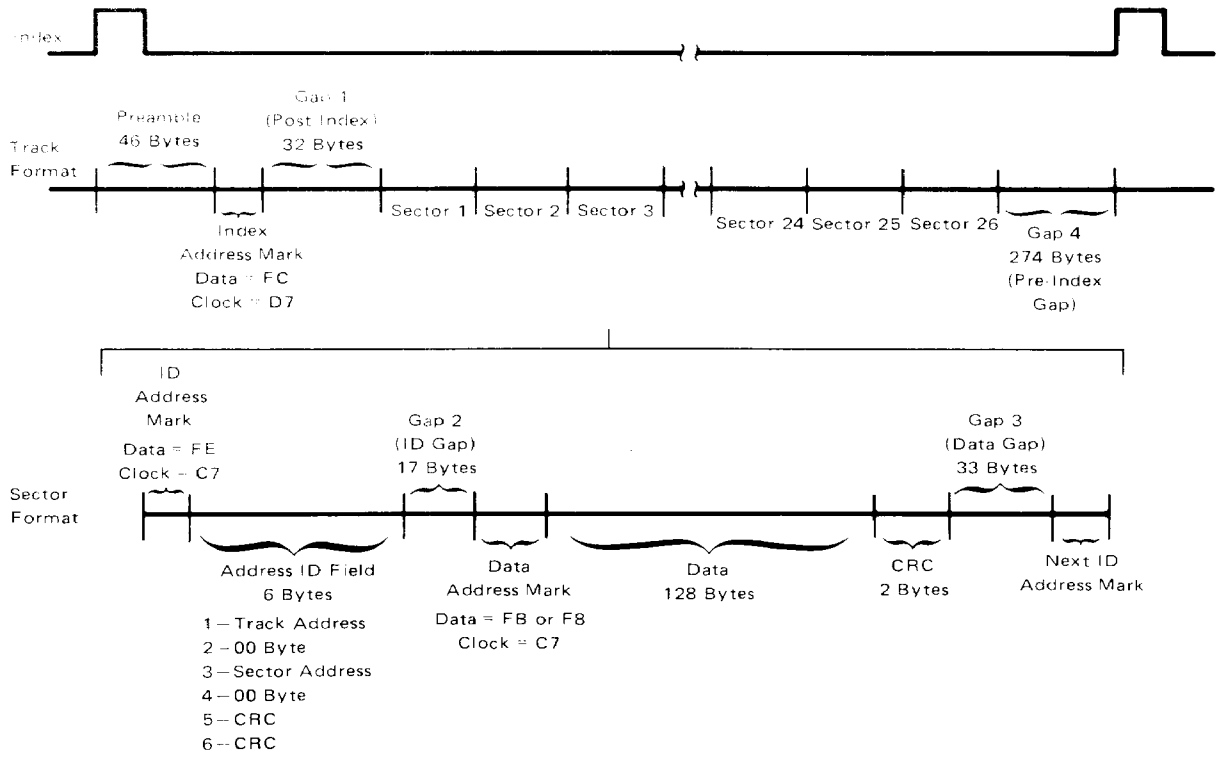


FIGURE 20 — SOFT SECTOR FORMAT



MACRO COMMAND SET

The macro command set shown in Table 4 is discussed in the following paragraphs.

Seek Track Zero (STZ)

The STZ command causes the R/W head to be released from the surface of the disk (HLD is reset) and positioned above track 00. The FDC issues step pulses on the STP output until the TRZ input becomes a high level or until 83 pulses have been sent to the drive. When the TRZ input becomes high, the step pulses are inhibited on the STP output but the FDC remains busy until all 83 have been generated internally.

If the TRZ input remains low (logic '0') after all 83 pulses have been generated, the Seek Error flag (STRB bit 4) is set.

After all 83 pulses have been generated, the head is loaded (HLD becomes a '1'). After the settling time specified in the SUR has expired, the Settling Time Complete flag is set (ISR bit 1), Busy (STRA-7) is reset, and CTAR and GCR are cleared. The head remains in contact with the disk. A command such as RCR (Read CRC) may be issued following a STZ if the head must be released.

Seek (SEK)

The SEK command is used to position the R/W head over the track on which a Read/Write operation is to be performed. The contents of the GCR are taken as the destination address and the contents of the CTAR is the source address; therefore, the number of pulses (N) on the STP output are given by:

$$N = |(CTAR) - (GCR)|$$

HDR is a '1' for (GCR) > (CTAR) otherwise it is a '0'.

When a SEK command is issued, Busy is set, the head is raised from the disk, HDR is set, and N number of pulses ap-

TABLE 4 — MACRO COMMAND SET

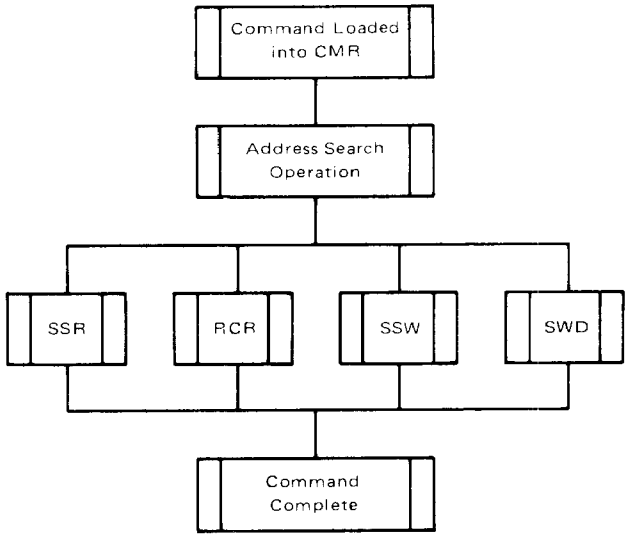
			CMR Bits				Hex
			Bit 3	Bit 2	Bit 1	Bit 0	Code
1	STZ	Seek Track Zero	0	0	1	0	2
2	SEK	Seek	0	0	1	1	3
3	SSR	Single Sector Read	0	1	0	0	4
4	SSW	Single Sector Write	0	1	0	1	5
5	RCR	Read CRC	0	1	1	0	6
6	SWD	Single Sector Write with Delete Data Mark	0	1	1	1	7
7	MSW	Multi Sector Write	1	1	0	1	D
8	MSR	Multi Sector Read	1	1	0	0	C
9	FFW	Free Format Write	1	0	1	1	B
10	FFR	Free Format Read	1	0	1	0	A

number of pulses appear on the STP output. After the last step pulse is used, the head is placed in contact with the disk. Once the head settling time has expired, the Settling Time complete flag (ISR bit 1) is set, Busy is reset, and the contents of the GCR are transferred to the CTAR.

SINGLE-SECTOR READ/WRITE COMMANDS

The single-sector Read/Write commands (SSR, RCR, SSW, and SWD) are used to Read/Write data from a single 128 byte sector on the disk. As shown in Figure 21 these types of instructions can be divided into two sections. The first section, which is common to all instructions, is the address search operation, while the second section is unique to the requirements of each instruction.

FIGURE 21 — BASIC SINGLE SECTOR COMMAND FLOW CHART



Address Search Operation

The flow chart of Figure 22 shows the operation of the address search.

Single-Sector Read (SSR)

The single-sector read command follows the address search procedure as defined in the previous flowchart. If the search is successful, status sense request is set and the operation continues as described by the flowchart of Figure 23.

Read CRC (RCR)

The RCR command is used to verify that correct data was written on a disk. The operation is the same as for the SSR command with the exception that the data-transfer request (STRA bit 0) is not set. The SSR interrupt can be disabled by using the DMA mode.

Single-Sector Write (SSW)

Single-sector write is used to write 128 bytes of data on the disk. After the command is issued, the address search is performed. The remainder of the instruction's operation is shown in Figure 24.

Single-Sector Write with Delete-Data Mark (SWD)

The operational flow of SWD is exactly like that of SSW. For SWD, the data pattern of the Data-Address Mark becomes F8 instead of FB. The clock pattern remains C7.

Multi-Sector Commands (MSR/MSW)

MSR is used for sequential reading of two or more sectors. If S sectors are to be read, S1 must be written into the GCR before the command is issued.

The basic operation for the MSR and MSW is the same as that for the SSR and SSW repsectively. The basic operation begins with an address search operation, which is followed by a single-sector read or write operation. This completes the operation on the first sector. The SAR is incremented, the GCR is decremented, and if no overflow is detected from the GCR (i.e., GCR becomes negative) the sequence is repeated until S number of sectors are read or written.

The completion of an MSR or MSW is like that of an SSR or SSW command. First MCC is set, after the settling time has expired, Busy is reset, and the head is released.

If a delete-data mark is detected during an MSR command, STRA bit 1 (Delete-Data Mark Detected) remains set throughout the commands operation.

When a multi-sector instruction is issued, the sum of the SAR and GCR must be less than 27. If SAR + GCR > 26, an address error (STRB bit 3 set) will occur after the contents of SAR becomes greater than 26.

Free-Format Write (FFW)

The FFW has two modes of operation which are selected by FWF (Free-Format Write Flag) which is data bit 4 of the CMR.

When the FWF = '0', the data bits of the DOR are written directly to the disk without first writing the preamble, address mark, etc. The contents of the DOR are FM modulated with a clock pattern of all ones.

If FWF = '1' the odd bits of the DOR are used as clock bits and even bits are used for data bits. In this mode, the DOSR clock is twice a normal write operation and one byte of DOR is one nibble (four bits of data) on the disk.

The two modes of the FFW command allow formatting a disk with either the IBM 3470 format or a user defined format.

After the FFW command is loaded into the CMR, WGT becomes a high level, the contents of DOR are transferred to the DOSR, data transfer request (STRA bit 0) is set, and the serial bit pattern is shifted out on the WDT line. Therefore, DOR must be loaded before the FFW command is issued. Data from the DOR is continually transferred to the DOSR and shifted out on WDT until the CMR has been written with an all zero pattern. When CMR becomes zero, WGT becomes a low level, but MCC is not set and the R/W head is left in contact with the disk.

Free-Format Read (FFR)

FFR is used to input all data (including Address Marks) from a disk. Once the FFR command is set into the CMR, the head is loaded and after the settling time has expired the serial data from the FDC is brought into the DISR. After 8 bits have accumulated, it is transferred to the DIR and Data-Transfer Request (STRA bit 0) is set.

FIGURE 22 – OPERATIONAL FLOW OF THE ADDRESS SEARCH SEQUENCE

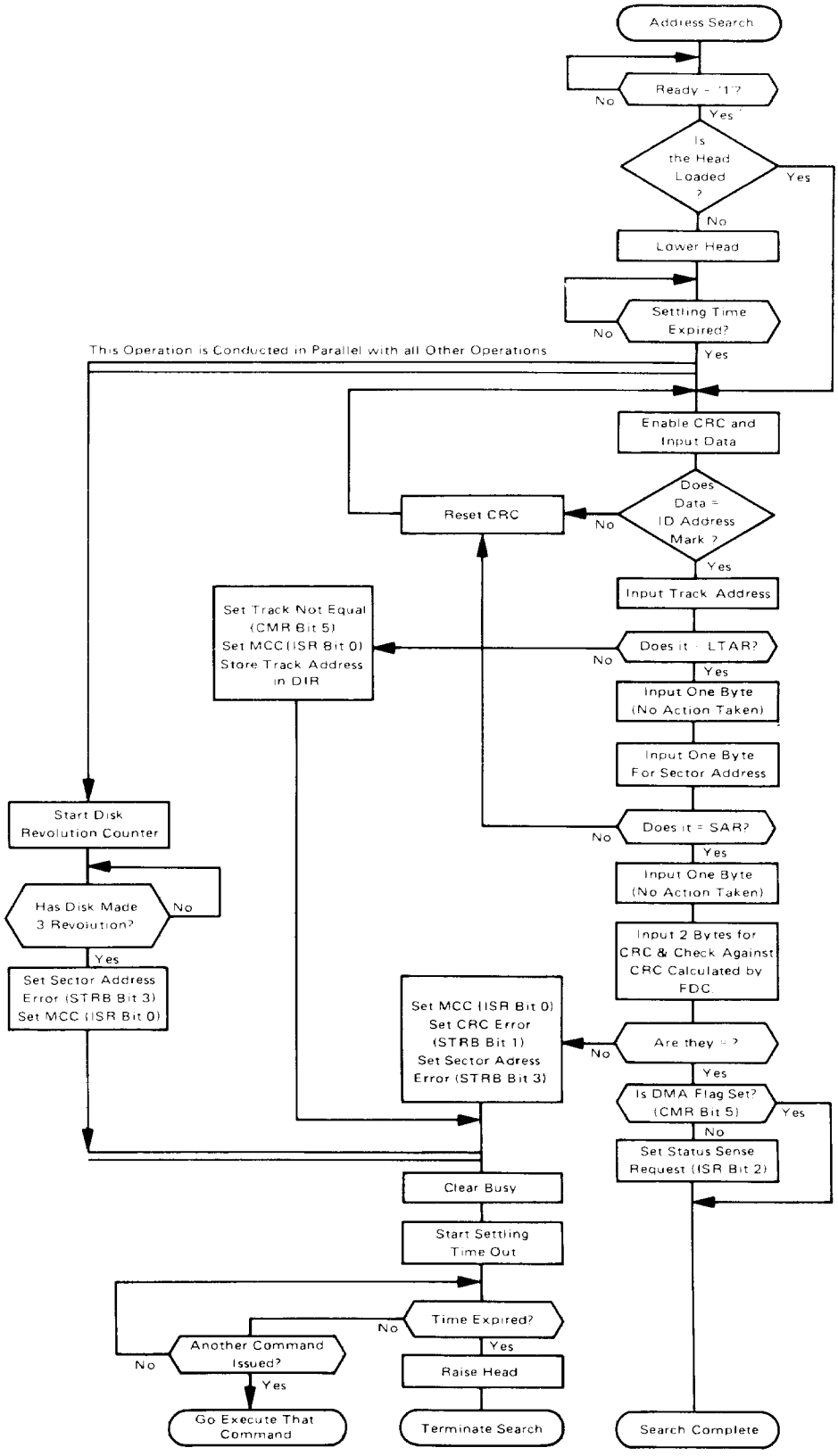


FIGURE 23 – OPERATIONAL FLOW OF THE SSR COMMAND

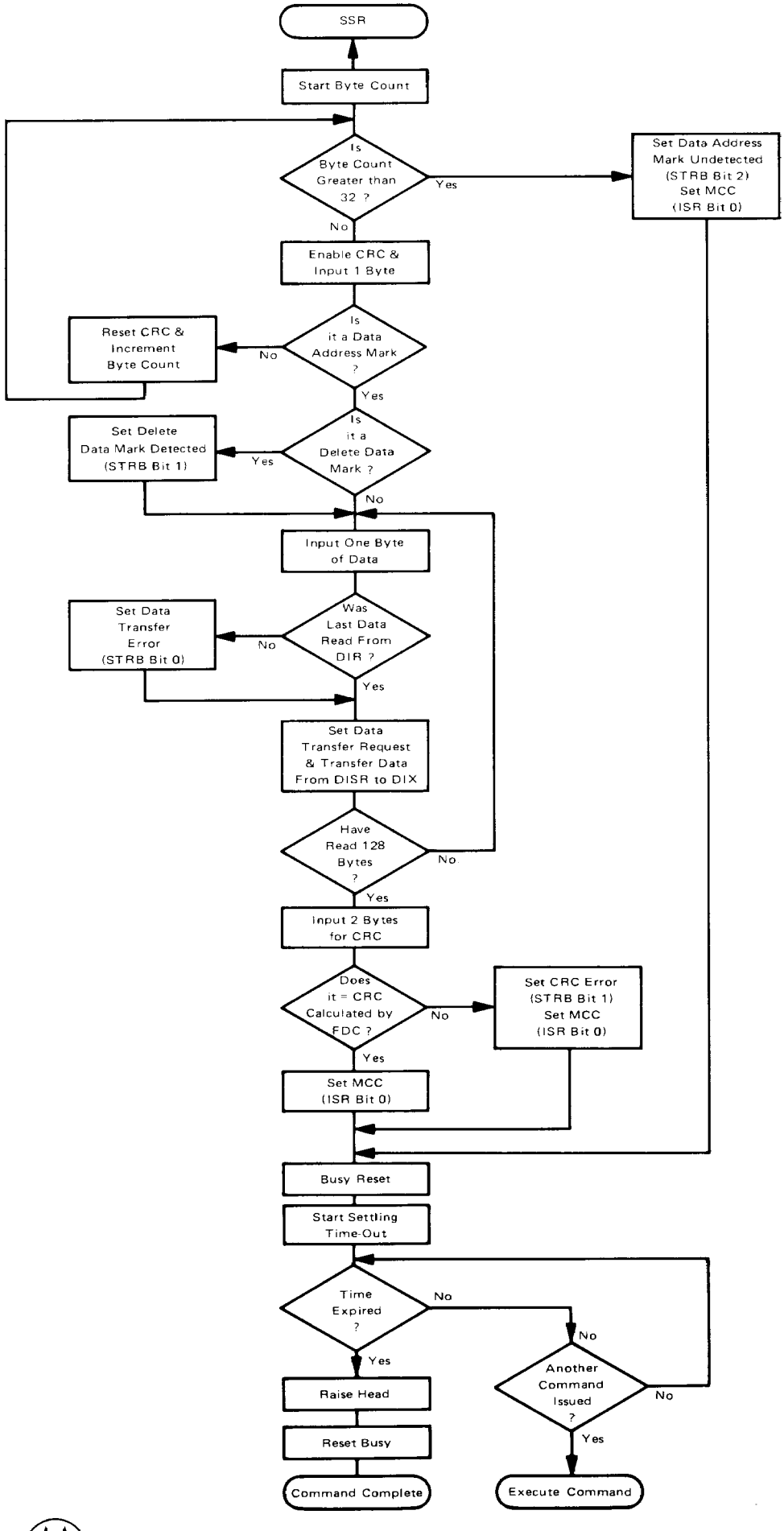
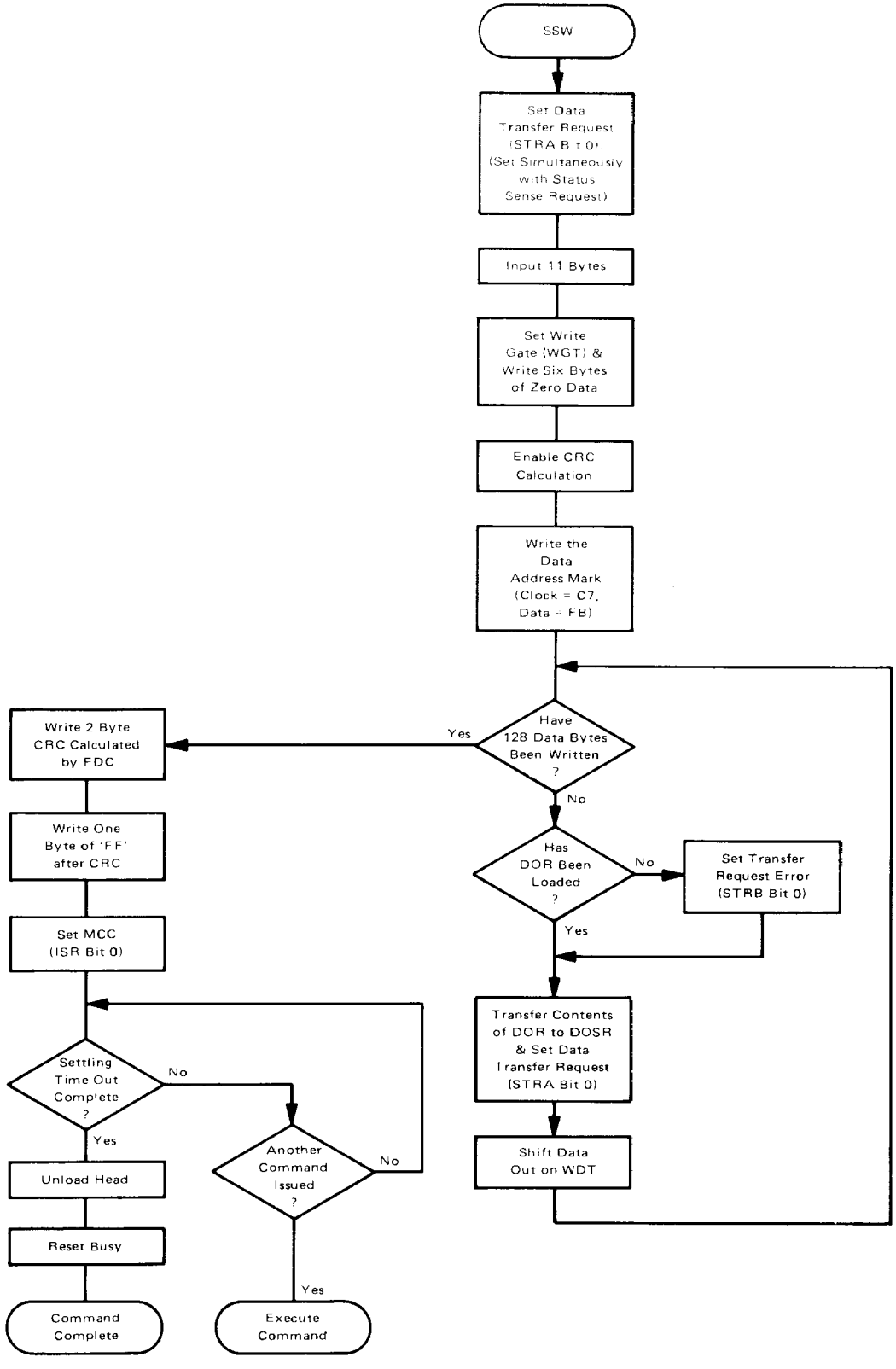


FIGURE 24 – OPERATIONAL FLOW OF THE SSW COMMAND



This operation continues until a zero pattern is stored in the CMR, terminating the FFR command. As in the case of the FFW command, MCC is not set and the head remains in contact with the disk.

The first data that enters the DISR is not necessarily the first bit of a data word since the head may be lowered at any place on the disk. To prevent the FDC from remaining unsynchronized to the data, the FFR command will synchronize to either an ID address mark (FE) or a Data-Address Mark (FB or F8).

REGISTER DEFINITIONS

DATA OUTPUT REGISTER (DOR)

Hex address 0, write only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8 Bits of Data Used for a Disk Write Operation							

When one of the four write macro commands (SSW, SWD, MSW, and FFW) is executed, the information contained in the DOR is loaded into the DOSR, and is shifted out on the WDT line using a double frequency (FM) format.

DATA INPUT REGISTER (DIR)

Hex address 0, read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
8 Bits of Data Used for a Disk Read Operation							

One of the three read macro commands (SSR, MSR, FFR) executed, will cause the information on the RDT input to be clocked into the DISR. When eight clock pulses have occurred, the eight bits of information in the DISR are transferred to the DIR where it can be read by the bus interface.

CURRENT TRACK ADDRESS (CTAR)

Hex address 1, read/write

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	7 Bit Track Address of Current Head Position						

The address of the track over which the R/W head is currently positioned is contained in the CTAR. At the end of a SEK command, the contents of the GCR are transferred to the CTAR. CTAR is cleared at the completion of a STZ command. CTAR is a read/write register so that the head position can be updated when several drives are connected to one FDC. Bit 7 is read as a '0'.

COMMAND REGISTER (CMR)

Hex address 2, write only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3*	Bit 2*	Bit 1*	Bit 0*
Function Interrupt Mask	ISR3 Interrupt Mask	DMA Flag	FWF	Macro Command			

*Bits 0-4 are clared by $\overline{\text{RESET}}$.

The commands that control the FDC are loaded into the lower four bits of the CMR. Information that controls the data transfer mode and interrupt conditions are loaded into bits 4 through 7.

Bit 0-Bit 3: Macro Command

The Macro Command to be executed by the FDC is written to bits 0-3.

Bit 4: Free-Format Write Flag (FWF)

If a Free-Format Write command is issued, the state of bit 4 of the CMR determines what clock source will be used. The FWF is defined in the FFW (Free-Format Write) command explanation.

Bit 5: DMA Flag

If bit 5 is a '1' the FDC is in the DMA mode. Bit 5 being a '1' inhibits setting of Status Sense Request (ISR bit 2) thereby preventing its associated interrupt. A logic '1' DMA flag also enables the TxRQ output allowing it to request DMA transfers when the Data Transfer Request flag (STRA bit 0) is set.

A logic '0' DMA flag indicates the program controlled I/O (PC I/O) mode is to be used.

Bit 6: ISR3 Mask

CMR bit 6 (ISR3 Mask) is used to control the operation of ISR bit 3. A logic '1' in CMR bit 6 inhibits ISR bit 3 from being set when STRB becomes non-zero. If CMR bit 6 (ISR3 Mask) is a '0' the ISR bit 3 will be set if any bit in STRB becomes set. The setting of ISR bit 3 will cause an interrupt if CMR bit 7 is a '0'.

Bit 7: Function Interrupt Mask

When CMR bit 7 is a logic '1' all interrupts are inhibited except Status Sense Request (ISR bit 2) which can only be inhibited by the DMA flag (CMR bit 5). A logic '0' in CMR bit 7 enables interrupts from ISR0 (Macro Command Complete) and ISR1 (Settling Time Complete), and if the ISR3 Mask is '0', from ISR3.

TABLE 5

Interrupt Status Register (Bits Causing Interrupts)	Command Register Masks That Affect Interrupts		
	CMR7 (Function Interrupt Mask)	CMR6 (ISR3 Mask)	CMR5 (DMA Flag)
ISR0 (Macro Command Complete)	M	X	X
ISR1 (Settling Time Complete)	M	X	X
ISR2 (Status Sense Request)	X	X	M
ISR3 (STRB Conditions)	M	M	X

X = No effect
M = Bits that are used as masks

INTERRUPT STATUS REGISTER (ISR)

Hex address 2, read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used (Read as '0')				STRB*	Status* Sense Request	Settling* Time Complete	Macro* Command

*Cleared by $\overline{RESET}$

Bit 0: Macro Command Complete

When an SSR, RCR, SSW, SWD, MSR or MSW Macro Command has completed execution, bit 0 bcomes set (logic '1'). If the function interrupts are enabled (bit 7 of CMR is a logic '0'), the conclusion of a Macro command's execution will cause an interrupt.

Bit 1: Settling Time Complete

Settling time complete is set on SEK and STZ commands to indicate the head has been loaded and the settling time specified in SUR has expired. Since MCC is not set for the SEK or STZ command, settling time complete can be used as an interrupt to signify the SEK or STZ command has finished. Settling Time Complete is not set for any of the R/W commands.

Bit 2: Status Sense Request

For an SSR, SSW, SWD, MSR, or MSW Command, Status Sense Request indicates that the specified address ID field has been detected and verified by a CRC check. This is used as an early indication that data transfers will occur after 18 more byte times. For MSR and MSW commands, it is set for each sector.

In the PC I/O mode, an interrupt occurs when Status Sense Request becomes a logic '1' regardless of the state of the CMR interrupt mask. In the DMA mode, (DMA flag of CMR is set) Status Sense Request is unchanged and does not generate an interrupt when the address ID field has been verified.

Bit 3: STRB

STRB is an 'OR' of all of the bits of Status Register B and is disabled by the STRB interrupt mask in the CMR (CMR bit 6). The equation:

$$STRB = CMR6 \cdot (STRB + STRB1 + STRB2 + STRB3 + STRB4 + STRB5 + STRB6 + STRB7)$$

describes the operation of Bit 3 of the ISR.

ISR0, ISR1, and ISR2 are cleared when the Interrupt Status Register is read, but ISR3 is cleared only after Status Register B has been read.

SET-UP REGISTER (SUR)

Hex address 3, write only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Track to Track Seek Time				Head Settling Time			

The SUR is not affected by a reset operation; therefore, once it is initialized, the information remains until power is removed from the FDC.

Bit 0-Bit 3: Head Settling Time

The head settling time is used to generate a delay after the head is placed in contact with the disk. This allows the head to stop bouncing before any operations are performed. The delay is programmed by bits 0-3 and is specified by the equation:

$$Delay = \frac{4096}{f} \cdot B$$

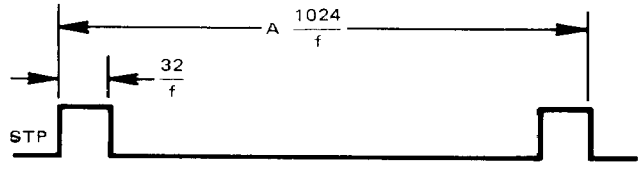
B = Number contained in bits 0-3 of SUR
f = Frequency of CLK input

For IBM 3740 compatibility f = 1 MHz and the timing range is 4.096 ms for a '0001' to 61.44 ms for a '1111'. A '0000' code prevents Settling Time complete from being set and the FDC must be Reset.

Bit 4-Bit 7: Track-to-Track Seek Time

The frequency of STP is determined by bit 4-bit 7 of SUR as shown below. If the track-to-track seek time is 0 the period of STP is 64/f.

A = Number specified in bits 4-7 of SUR
f = Frequency of clock input



A = Number specified in bits 4-7 of SUR.
f = Frequency of clock input.

For IBM compatible operation, f is 1 MHz. This results in an STP pulse width of 32 μs and an STP interval of 1.024 ms for 0001 in bits 7-4 to 15.36 ms for 1111.

STATUS REGISTER A (STRA)

Hex address 3, read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Busy*	Index	Track* Not Equal	Write Protect	Track Zero	Drive Ready	Delete* Data Mark Detected	Data* Transfer Request

*Cleared by $\overline{RESET}$

Bit 0: Data Transfer Request

For a write operation (SSW, SWD, MSW, FFW) the transfer request bit indicates that the DOR is ready to accept the next data word to be written on the disk. If data is not written into the DOR before the last data bit in the DOSR is shifted out to the WDT line, the data transfer error bit (bit 0 of STRB) will be set. After a write command has been issued, the first transfer request occurs simultaneously with the Status Sense Request. For a write operation, transfer request is reset after the DOR has been written from the data bus.

During a read operation (SSR, MSR, FFR) the transfer request bit signifies data from the DISR has been transferred to the DIR. The DIR must be read before the DISR is full again or the data transfer error bit (bit 0 of STRB) will be set. For read operations, transfer request is reset by a read of the DIR.

Bit 1: Delete Data Mark Detected

A Single-Sector Read operation that detects a delete data code (F8), instead of a general code (FB) as a Data Address Mark, will set the Delete Data Mark Detected bit. For the MSR command, bit 1 is set the first time an 'F8' code is found and remains set throughout the execution of the command. Bit 1 is reset whenever an SSR, SSW, SWD, MSR, MSW, or RCR command is issued.

Bit 2: Drive Ready

The Drive Ready bit indicates the state of the Ready input from the floppy disk drive. If a command is issued with Ready at logic '0', its execution will be inhibited until Ready becomes a logic '1'. If ready becomes a '0' during the execution of a command the Hard Error Flag (STRB bit 7) is set.

Bit 3: Track Zero

The state of the Track Zero input from the floppy disk drive is reflected in this bit of STRA. A logic '1' on the Track Zero input inhibits step pulses during an STZ command.

Bit 4: Write Protect

The Write Protect input from the floppy disk drive is reflected by bit 4 of STRA. A high level (logic '1') on the WPT input during the execution of any write command results in a write error (bit 6 of STRB set).

Bit 5: Track Not Equal

If the track address read from the address ID field does not coincide with the address in the LTAR, the Track Not Equal bit is set. Track Not Equal applies to all non-free format read/write commands, and is reset after a non-free format read/write command is issued.

Bit 6: Index

The state of the index input appears in bit 6 of STRA. The index input is used to count the number of disk revolutions while the FDC is looking for the address ID field (see operation of STRB bit 3) during the address search phase of a non-free format read/write command.

Bit 7: Busy

When Busy is a logic '1', the FDC is executing a command and no new commands can be issued.

SECTOR ADDRESS REGISTER (SAR)

Hex address 4, write only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used			5 Bit Sector Address				

Before a data transfer macro command (SSW, SWD, SSR, RCR, MSW, MSR) is issued, the address of the sector on which the operation is to be performed must be written into the SAR. The address in the sector address byte of an Address ID field of the disk is compared with the contents of the SAR. During an MSW or MSR command, the SAR is incremented after each sector is read or written. When execution is complete, the SAR contains the address of the last sector on which an operation was performed plus one. At the completion of an STZ or SEK command, SAR is cleared.

STATUS REGISTER B (STRB)

Hex address 4, read only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hard* Error	Write* Error	File Inoperable	Seek* Error	Sector* Address Undetected	Data* Mark Undetected	CRC* Error	Data* Transfer Error

*Cleared by $\overline{\text{RESET}}$

The bits of the STRB represent possible error conditions that may occur during execution of macro commands. Whenever STRB is reset, ISR bit 3 is also reset.

Bit 0: Data Transfer Error

Data Transfer indicates an underflow or overflow of data. If a Write operation is being performed, it signifies that data was not presented to the DOR before the DOSR became empty. In this case, the current contents of the DOR are transferred to the DOSR and the write operation continues. The data transfer error remains set until data is written into the DOR. The operation of the CRC is unchanged.

For read commands, a data transfer error indicates that data in the DIR was not read before the next data word from the disk was transferred to the DIR. The read operation continues until sufficient data has been read from the disk to satisfy the requirements of the command (128 bytes for SSR). The error indication remains set until STRB is read, and the transfer request remains set until data is read from the DIR.

Bit 1: CRC Error

A CRC error occurs when the CRC read from the disk does not match that calculated by the FDC on the data it reads from the disk. A CRC error can occur in three different situations; checking the address ID field, checking the data field, and checking the FFR data. (See operation of CCR.)

If the CRC error occurs during the check of an address ID field, Sector Address Undetected (STRB bit 3) will also be indicated (see Table 6). A CRC error of a data field is indicated by a CRC error and no sector address error.

Bit 2: Data Mark Undetected

If a valid mark is not detected in the data block of a sector, it is indicated by a Data Mark Undetected error. Data Mark Undetected is reset after a non-free format Read/Write command is issued.

Bit 3: Sector Address Undetected

The sector address bit can be set on two conditions; not finding the sector address and a CRC error on an address ID field.

If the disk makes three revolutions during an address search operation and the sector address specified in the sector address register is not found in any of the address ID fields, a sector address undetected condition is indicated.

A CRC error that occurs on an address ID field will set bit 3 also. Table 6 shows how bits 1 and 3 are related.

TABLE 7 — PROGRAMMING REFERENCE DATA

Table 7 is a summary of the information in the data sheet and can be used as a reference when programming the MC6843.

Registers	Hex Address	R/$\overline{W}$ Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR	0	WO	8 Bits of Data Used for a Disk Write Operation							
DIR	0	RO	8 Bits of Data Used for a Disk Read Operation							
CTAR	1	R/W	Not Used	7 Bit Track Address of Current Head Position						
CMR	2	WO	Function Interrupt Mask	ISR3 Interrupt Mask	DMA Flag	FWF	* Macro Command	*	*	*
ISR	2	RO	Not Used				* STRB	Status Sense Request *	Settling Time Complete *	Macro Command Complete *
SUR	3	WO	Track to Track Seek Time				Head Settling Time			
STRA	3	RO	* Busy	Index	Track Not Equal *	Write Protect	Track Zero	Drive Ready	Delete Data Mark Detected *	Data Transfer Request *
*SAR	4	WO	Not Used			5 Bit Sector Address				
STRB	4	RO	Hard Error *	Write Error *	File Inoperable	Seek Error *	Sector Address Undetected *	Data Mark Undetected *	CRC Error *	Data Transfer *
GCR	5	WO	Not Used	7 Bit Count for Track Number on SEK or Sector Count for MSR or MSW.						
CCR	6	WO	Not Used						Shift CRC	CRC Enable
LTAR	7	WO	Not Used	7 Bit Search Track Address						

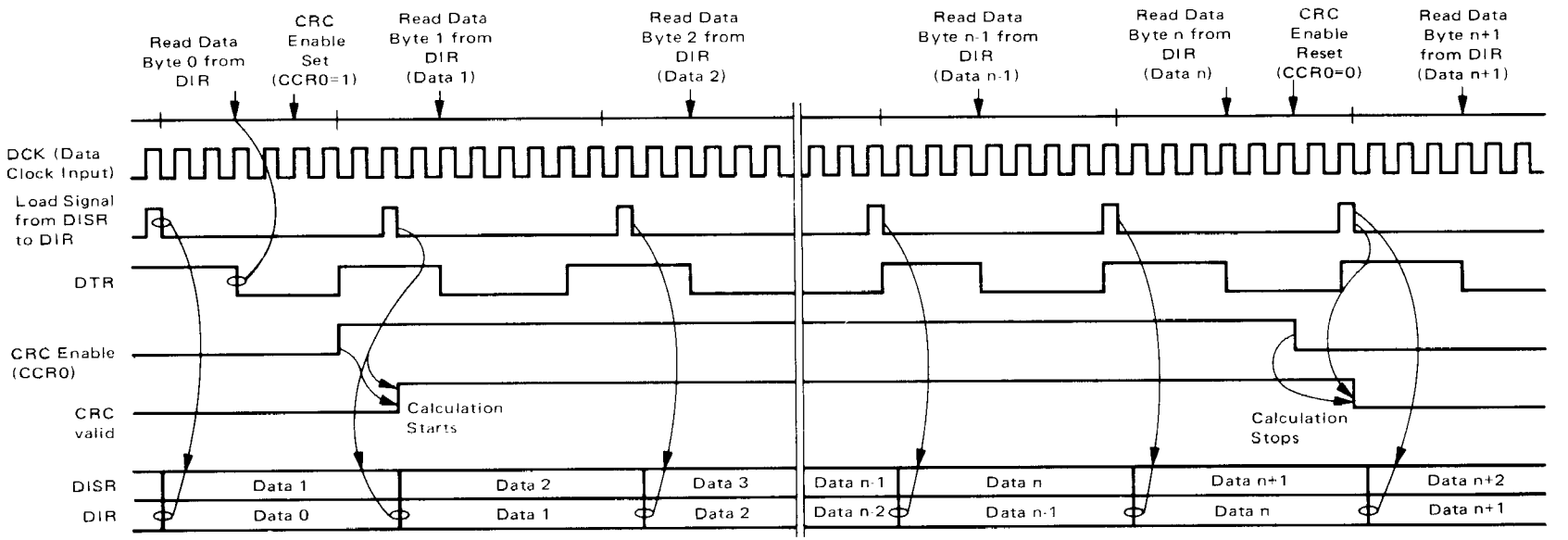
RO — Read Only
WO — Write Only
R/W — Read/Write

*Cleared by Reset

MACRO COMMANDS

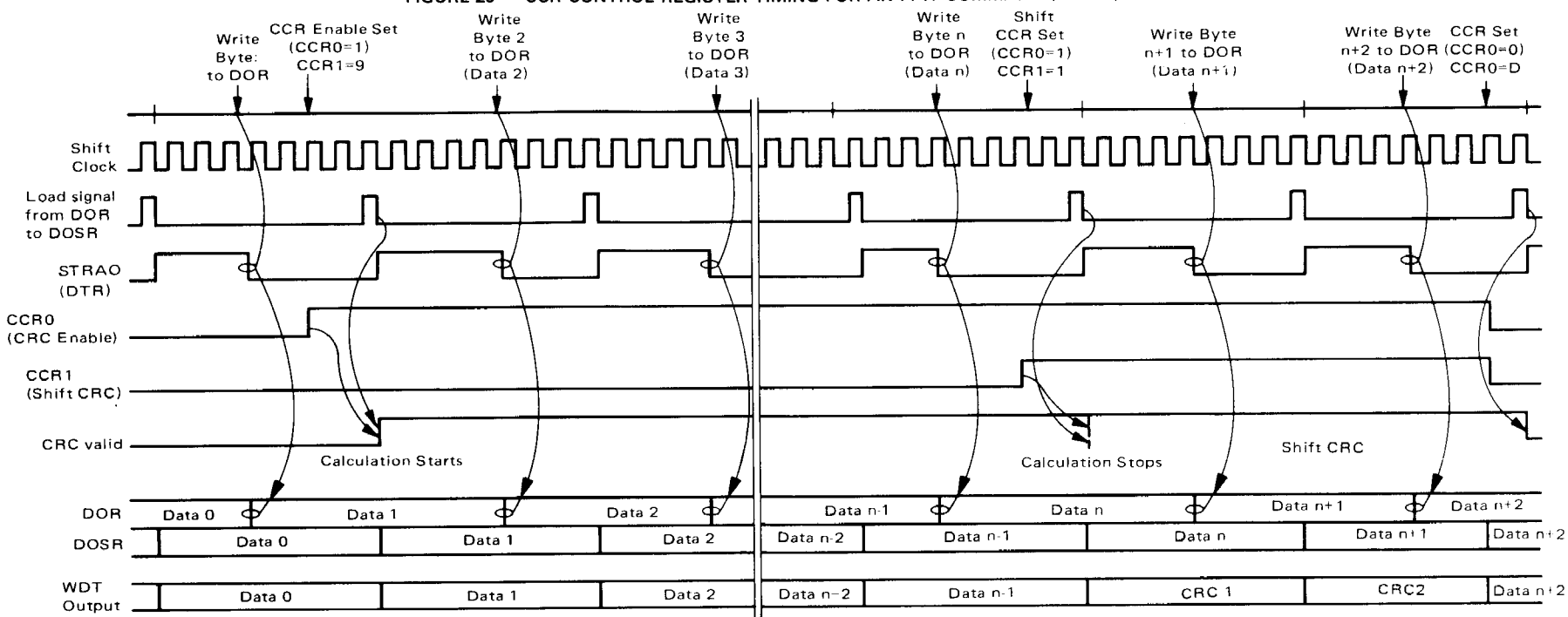
Hex Code	Instruction	Hex Code	Instruction
2	STZ	A	FFR
3	SEK	B	FFW
4	SSR	C	MSR
5	SSW	D	MSW
6	RCR		
7	SWD		

FIGURE 25 — CCR CONTROL REGISTER TIMING FOR AN FFR COMMAND (READ)



CRC Calculation includes Data Byte 1 through Data Byte n.

FIGURE 26 — CCR CONTROL REGISTER TIMING FOR AN FFW COMMAND (WRITE)



The CRC Calculation includes Data Byte 1 through Data Byte n-1.

TABLE 6 — RELATIONSHIP OF CRC ERROR AND SECTOR ADDRESS UNDETECTED

CRC Error (STRB 1)	Sector Address Undetected (STRB 3)	Condition
0	0	No Error
0	1	Sector Address not Detected
1	0	CRC Error on a Data Field
1	1	CRC Error on Address ID Field

Bit 4: Seek Error

An STZ (Seek Track Zero) command that never receives a track zero indication on the track zero input will result in a Seek Error (see description of STZ command).

Bit 5: File Inoperable

The state of the File Inoperable input appears in bit 5. If the File Inoperable input is a '1', a pulse of width 1/f (where f = Frequency of the clock input) is issued on the FIR output when STRB is read. FI is not latched but the input is gated to the bus when STRB is read.

Bit 6: Write Error

If the WPT input becomes a high level (logic '1') during the execution of a write command the write error bit is set.

Bit 7: Hard Error

If the Ready input becomes a '0' during the operation of a command (Busy is set), a hard error indication will result.

GENERAL COUNT REGISTER (GCR)

Hex address 5, write only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	7 Bit Count for Track Number on SEK Command and Sector Count for MSR or MSW Command						

The GCR contains the destination track address for the R/W head on an SEK Macro Command. The contents of the GCR are transferred to the CTAR at the end of the SEK Command. For multi-sector read or write operations (MSR, MSW), the GCR contains the number of sectors to be read minus one. During the MSR or MSW execution the GCR is decremented after each sector is read or written.

CRC CONTROL REGISTER (CCR)

Hex address 6, write only

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used						Shift CRC	CRC Enable

The CCR information is used only in the free format commands; for all other commands this register is masked and has no function.

Bit 0: CRC Enable

During an FFW command, CRC Enable is set by software and CRC generation takes effect on the next transfer of data from DOR to DOSR (see Figure 25). The CRC generation continues until Shift CRC (CCR bit 1) is set.

For an FFR command, CRC Enable is set by software and CRC generation takes effect on the next data read from DIR. The calculation continues for all data bytes read from DIR until CRC Enable is reset. The bytes read previous to resetting CRC Enable are considered the CRC information bytes and the CRC check is made against them.

Bit 1: Shift CRC

Bit 1 is valid only for the FFW command. After setting, it takes effect on the next transfer of data from DOR to DOSR (see Figure 26). Setting Shift CRC terminates the CRC calculation and causes the CRC calculated on all the data written into DOR up to the setting of bit 1, to be shifted out the WDT output. The CRC calculation will not include any data written to DOR after Shift CRC is set.

LTAR (LOGICAL TRACK ADDRESS)

Hex address 7, write only

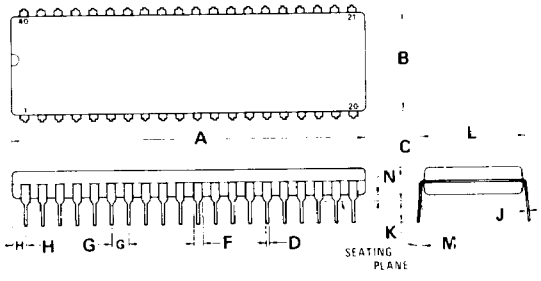
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not Used	7 Bit Logical Track Address						

When a read or write macro command (SSW, SWD, SSR, RCR, MSW, MSR) is issued, the address of the track on which the operation is to be performed must be written into the LTAR. The address in the track address byte of an Address ID field of the disk is compared with the contents of the LTAR. The contents of LTAR are not affected by the execution of any of the commands.

TABLE 8

Table 8 is a list of all error flags showing what conditions will cause the error, the instructions for which they are valid, and what conditions reset them.

Name	Flag	Set Condition	Reset Condtiion	Command
Track Not Equal	STRA5	The track address that is read from the disk does not coincide with the content of the LTAR.	Upon issuance of SSW, SSR, SWD, RCR, MSR, MSW command	SSW, SSR, SWD, RCR, MSR, MSW
Data Transfer Error	STRB0	During the data transfer between the drive and the MPU or memory, an overrun or underflow occurs.	Reading of STRB	SSW, SSR, SWD, RCR, MSR, MSW, FFR, FFW
CRC Error	STRB1	In checking the CRC of an ID field or a Data field, a CRC error occurs.	Reading of STRB	SSW, SSR, SWD, RCR, MSR, MSW, (FFR)
Data Mark Undetected	STRB2	If data address mark (FB or F8) is not detected within 32 bytes after the address ID field has been detected.	Upon issuance of SSW, SSR, SWD, RCR, MSR, MSW Command	SSR, RCR, MSR
Sector Address Undetected	STRB3	(1) The sector address that coincides with the contents of the SAR does not exist on the track. (2) A CRC error occurs in checking the ID field.	Reading of STRB	SSW, SSR, SWD, RCR, MSR, MSW
Seek Error	STRB4	During a STZ command, the TKZ input remains low after 83 pulses have been issued on the STP output.	Reading of STRB	STZ
FI	STRB5	File Inoperable input is high.	Reading STRB causes the FIR output to go High. This should reset the FI input.	SSW, SWD, MSW, FFW
Write Error	STRB6	The WPT input is high, and a write operation is executed.	Reading of STRB with either WGT or WPT reset.	SSW, SWD, MSW, FFW
Hard Error	STRB7	During the execution of command (Busy is 1) the RDY input becomes low.	Reading of STRB	All commands



CASE 711-02
(PLASTIC)

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.82	52.32	2.040	2.060
B	13.72	14.22	0.540	0.560
C	4.57	5.08	0.180	0.200
D	0.36	0.51	0.014	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	3.05	3.56	0.120	0.140
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "D").
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.